

# COMPAL CONFIDENTIAL

MODEL NAME : ADM60

PCB NO : DAA000AD000

BOM P/N : 4319XY31L01/L02

## Park City 12" UMA

**Skylake U**

2015-09-25

REV : 1.0 (A00)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

X76@ : SATA REDRIVER OPTION

MB PCB

Part Number	Description
DAA000AD000	PCB 12K LA-C621P REV0 MB

Layout Dell logo



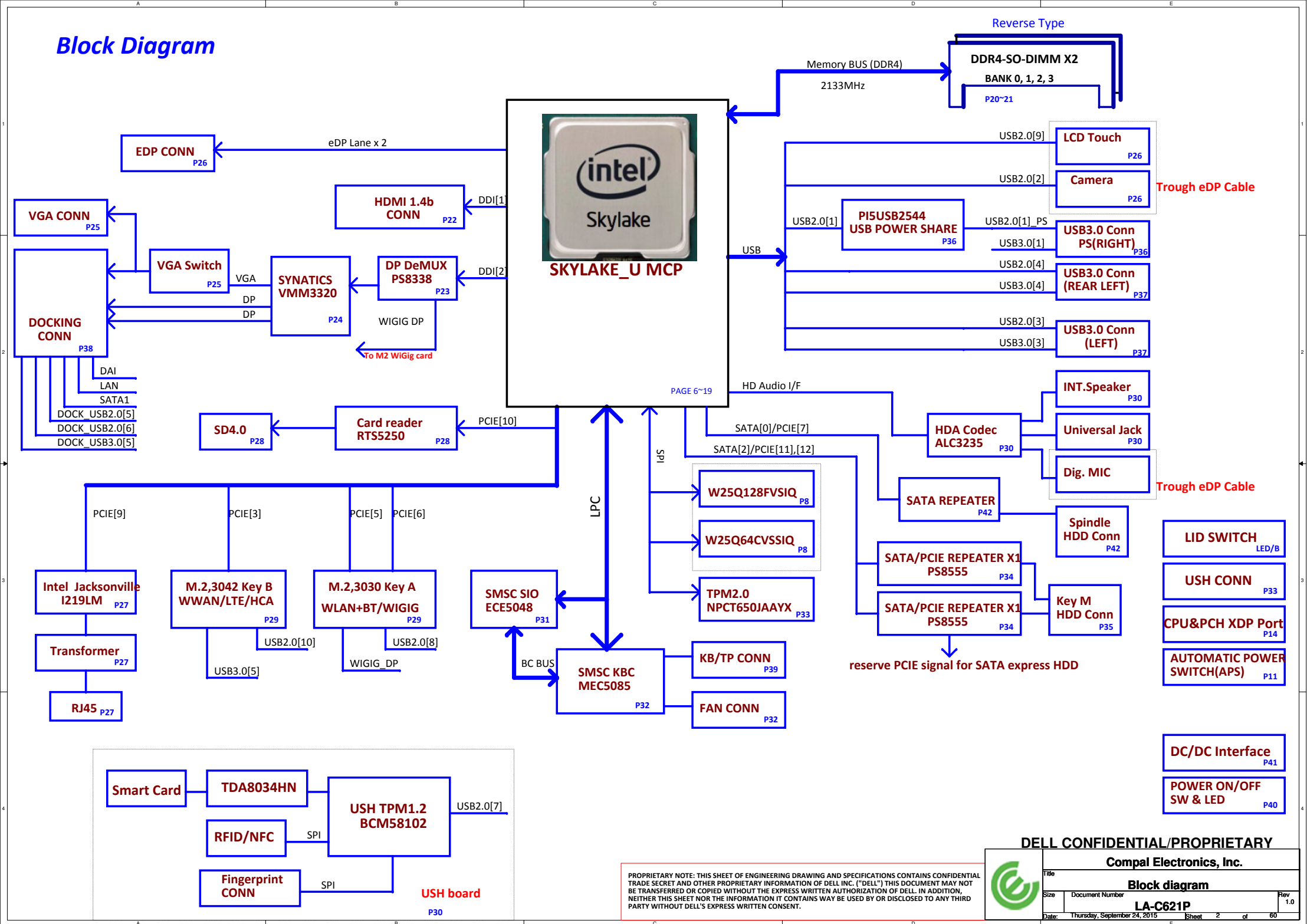
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# Block Diagram



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## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

## PM TABLE

State	power plane	(M-OFF)
S0	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.5V_RUN +3.3V_M +3.3V_M +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA
S3	ON	ON
S5 S4/AC	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	TU662	0.5
			Add Plating		
1	Top	3.7	Copper foil	0.5oz+plating	1.8
2	GND	3.7	Prepreg	1080	1.8
3	IN 1	3.7	Copper foil	1oz	1.25
4	GND/PWR	3.8	Core	4mil	3.87
5	IN 2	3.7	Copper foil	1oz	1.25
6	IN 3	3.7	Prepreg	2116H	1.25
7	GND/PWR	3.7	Copper foil	1oz	1.25
8	IN 4	3.8	Core	4mil	3.87
9	GND	3.7	Copper foil	1oz	1.25
10	Bottom	3.7	Prepreg	1080	1.8
			Add Plating	0.5oz+plating	1.8
			SolderMask	TU662	0.5
Overall Thickness (1.2mm ± 10%)					48.28000
					1.226312

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USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Right
USB3.0-2	SSIC-1			EDOCK PORT1
USB3.0-3	SSIC-2			JUSB1-->LEFT
USB3.0-4				JUSB2-->Rear LEFT
USB3.0-5		PCIE-1		M2 3042(WWAN)
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3042(HCA or QCA LTE)
		PCIE-4		NA
		PCIE-5		M.2 3030(WLAN)
		PCIE-6		M.2 3030(WIGIG)
		PCIE-7	SATA-0	HDD SATA
		PCIE-8	SATA-1	EDOCK E-SATA
		PCIE-9		LOM
		PCIE-10		Card Reader
		PCIE-11	SATA-1*	M.2 Socket 3 (Key M) (PCIex2 or SATA)
		PCIE-12	SATA-2	

USB PORT#	DESTINATION
1	JUSB1-->Right
2	Camera
3	JUSB2-->LEFT
4	JUSB3-->Rear LEFT
5	EDOCK PORT1
6	EDOCK PORT2
7	USH
8	M.2 304230(BT)
9	Touch Screen
10	M2 3042(WWAN)

USH	0	BIO
	1	NA

Check

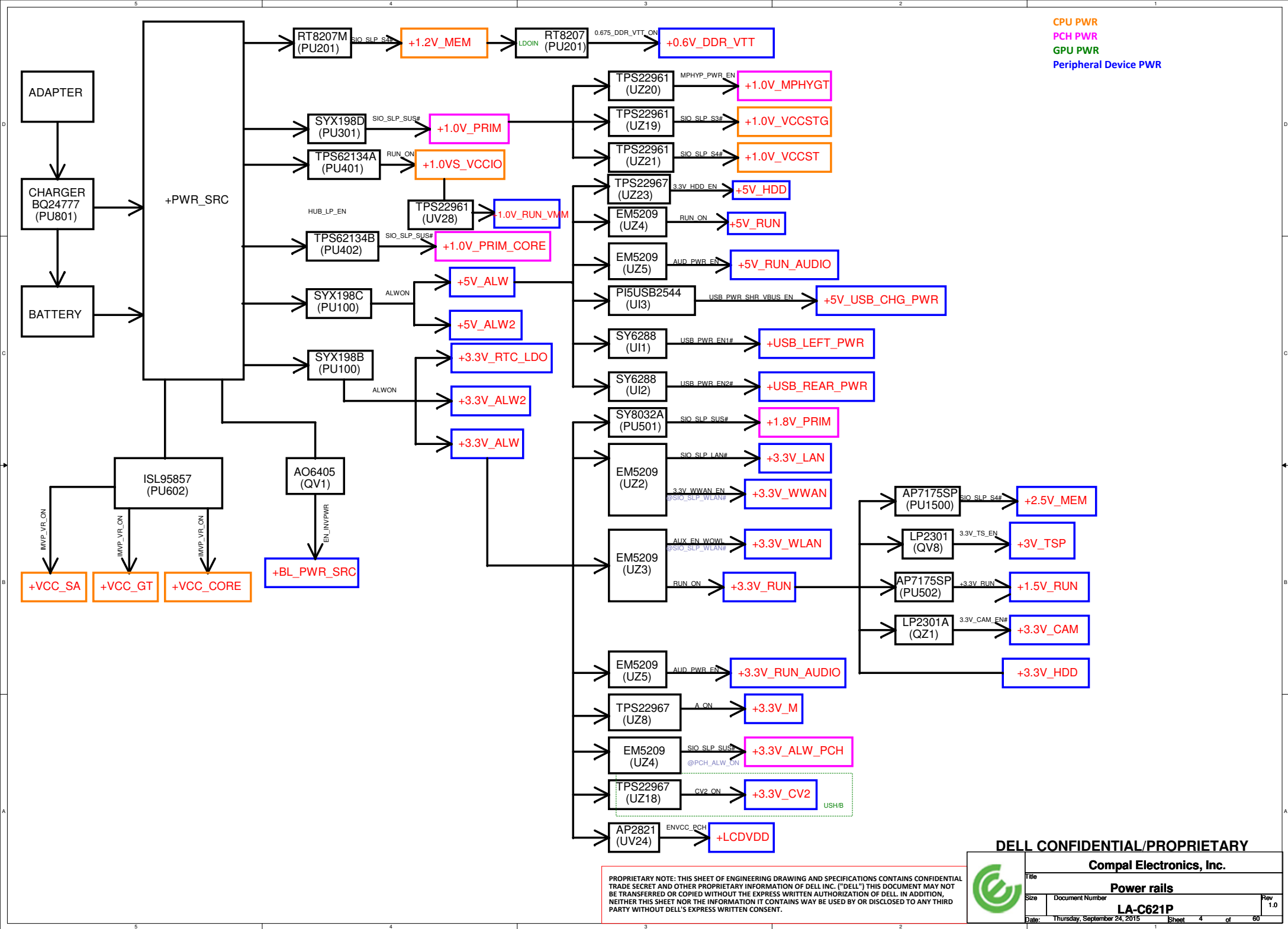
## High Speed I/O (HSIO) Lane Multiplexing in SKL U

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
USB3 # 1 (Capable of OTG)	USB3 # 2	USB3 # 3	USB3 # 4	USB3 # 5	USB3 # 6	PCIE # 3	PCIE # 4	PCIE # 5	PCIE # 6	PCIE # 7	PCIE # 8	PCIE # 9	PCIE # 10	PCIE # 11	PCIE # 12
				PCIE # 1	PCIE # 2		GbE	GbE	GbE	SATA # 0	SATA # 1	GbE	GbE	SATA # 1*	SATA # 2
							X4	X4	X4	X4	X4	X4	X4	X4	X4
							X2	X2	X2	X2	X2	X2	X2	X2	X2

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Port assignment			
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### DDR4, Ballout for side by side(Non-Interleave)

## DDR4 COMPENSATION SIGNALS

**CAD Note:**  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

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Title **CPU (2/14)**

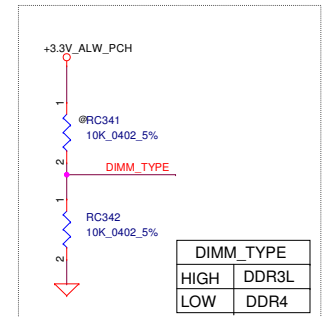
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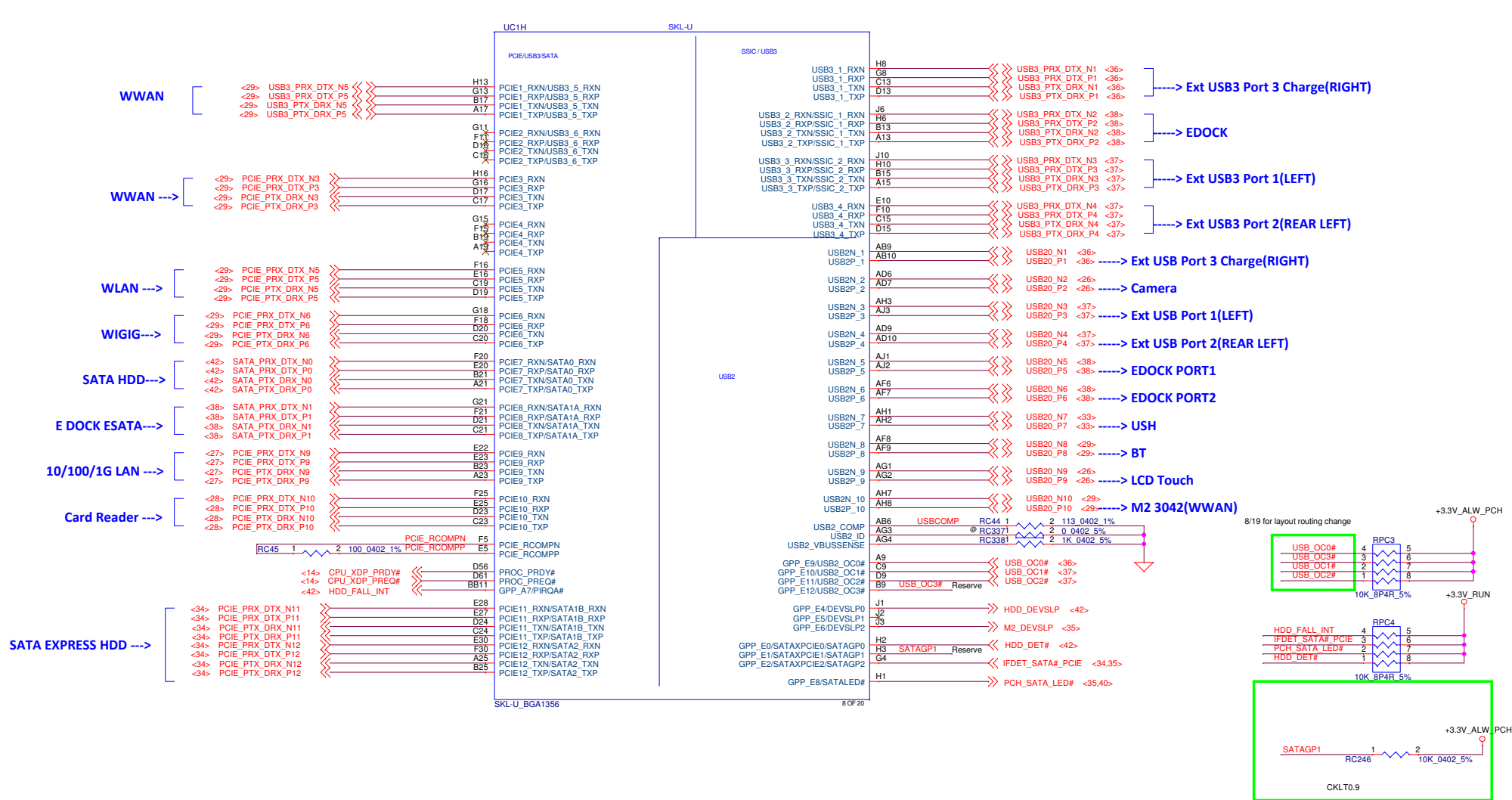
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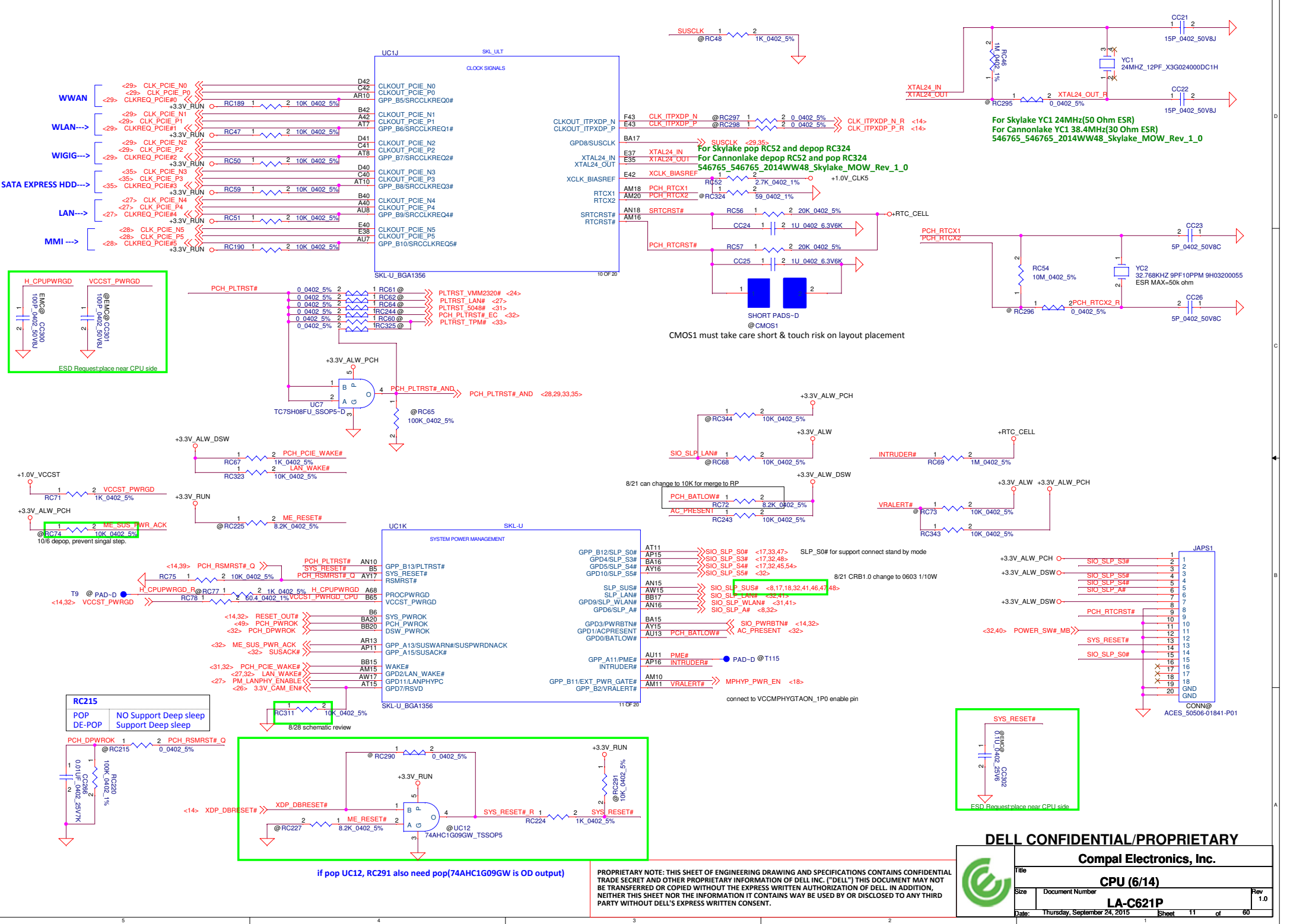
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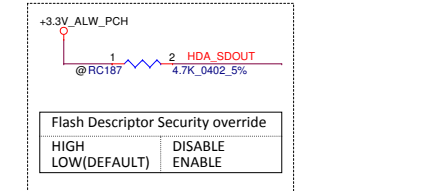
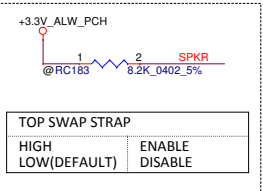
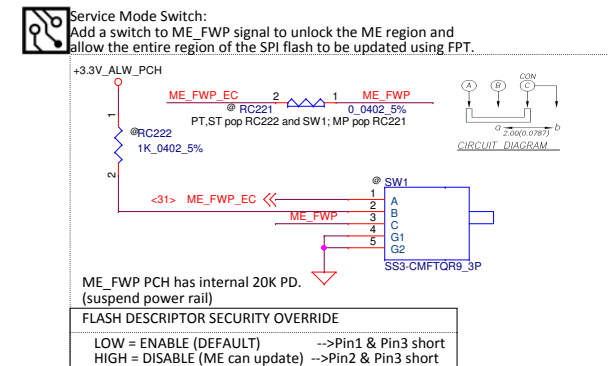
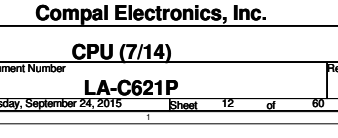
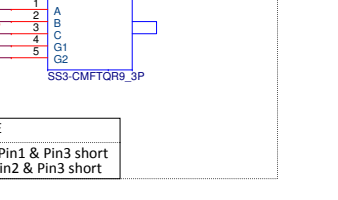
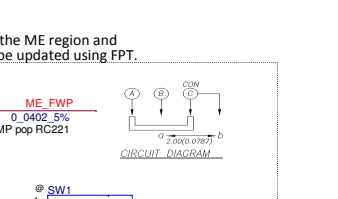
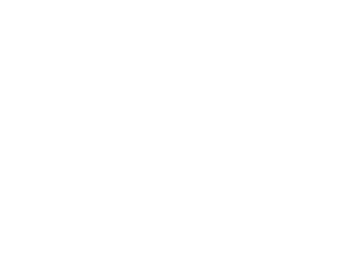
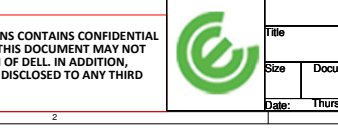
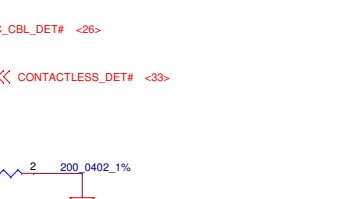
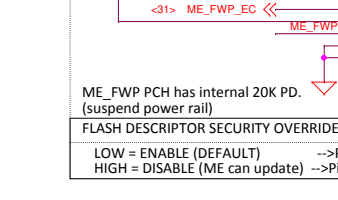
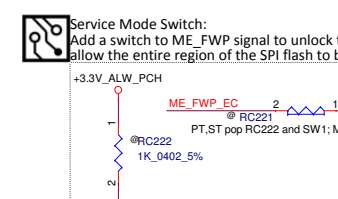
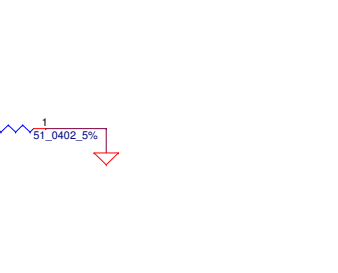
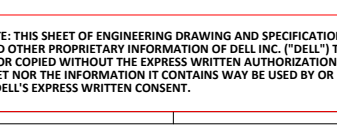
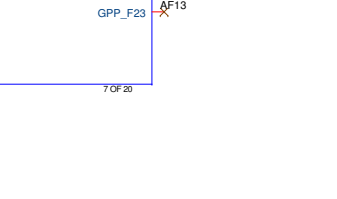
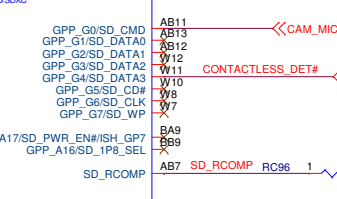
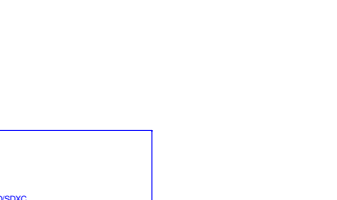
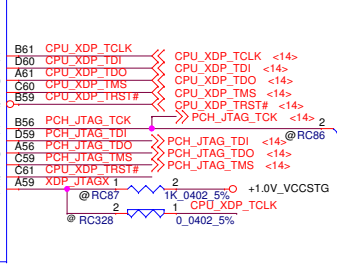
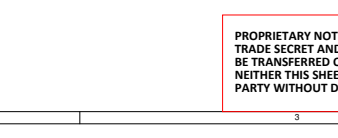
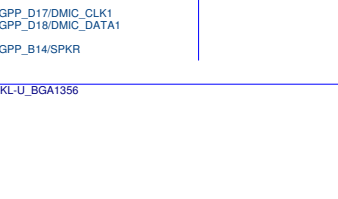
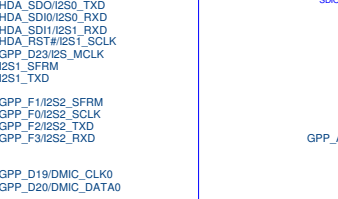
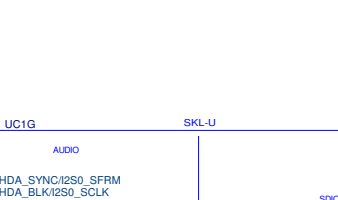
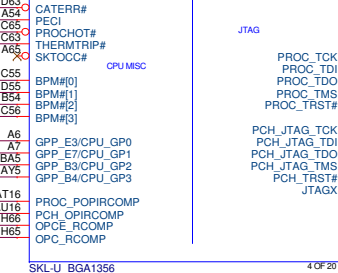
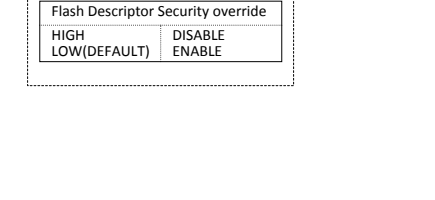
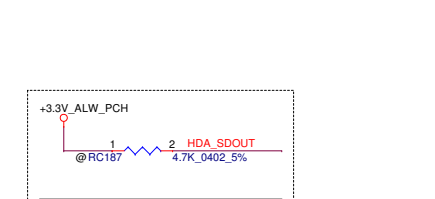
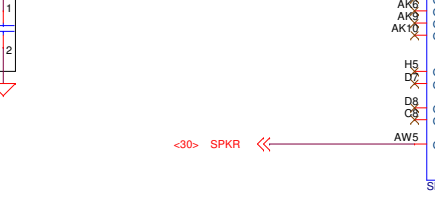
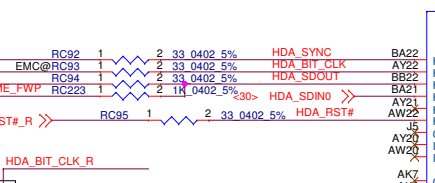
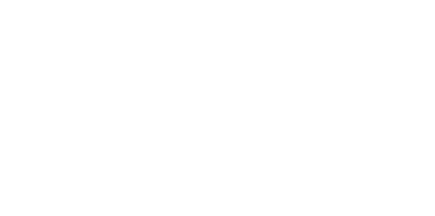
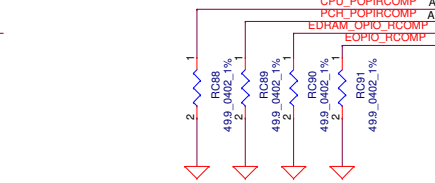
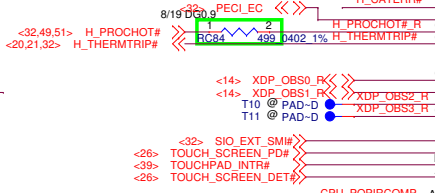
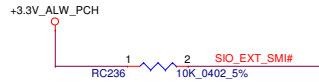
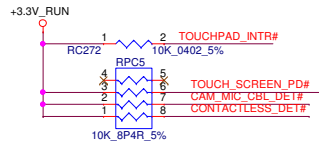
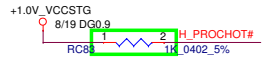
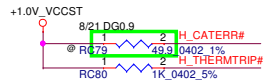
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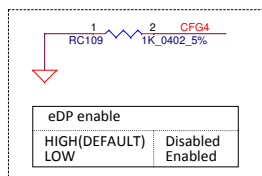
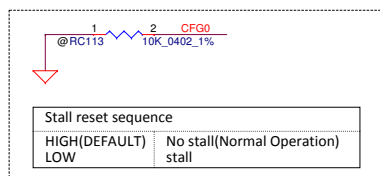
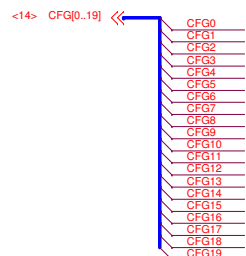
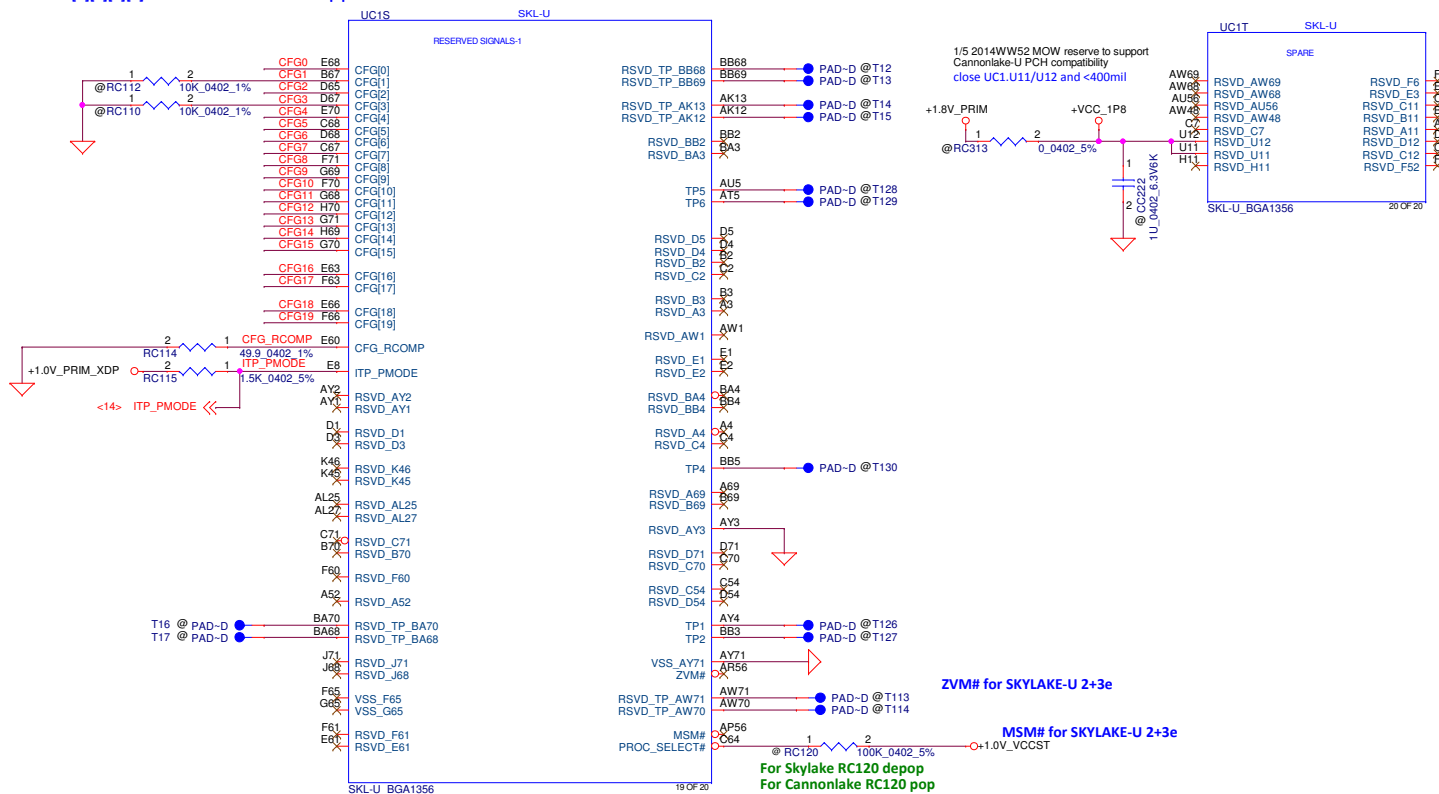
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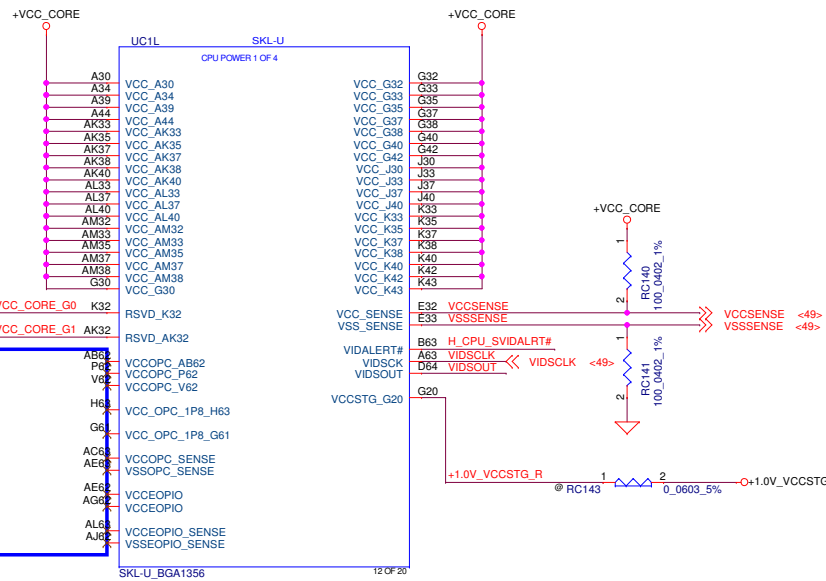
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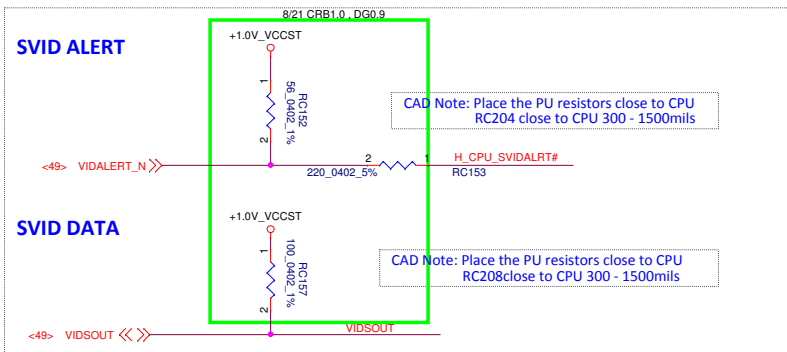
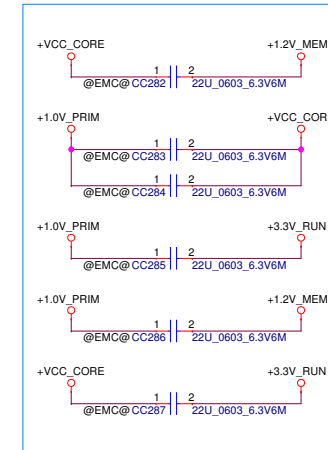
+VCC\_CORE: 0.3~1.35V



PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:  
Package edge > 0402 caps > 0805 caps > Power source

### ESD Request



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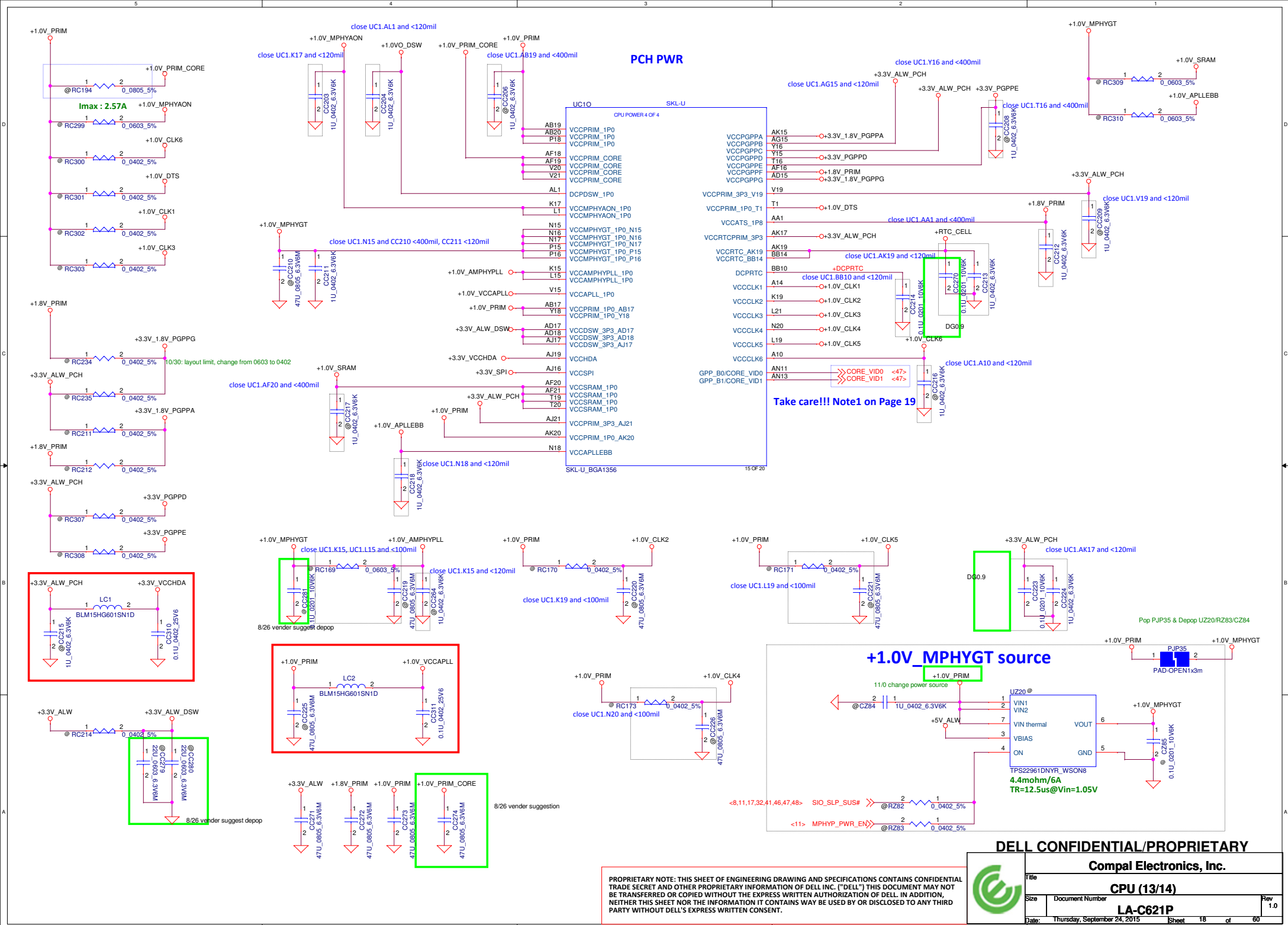
UC1M		SKL-U	
CPU POWER 2 OF 4			
A48	VCCGT	N70	
A53	VCCGT	N71	
A58	VCCGT	R63	
A62	VCCGT	R64	
A66	VCCGT	R65	
AA63	VCCGT	R66	
AA64	VCCGT	R68	
AA66	VCCGT	R69	
AA67	VCCGT	R70	
AA69	VCCGT	R71	
AA70	VCCGT	T62	
AA71	VCCGT	U65	
AC64	VCCGT	U68	
AC65	VCCGT	U71	
AC66	VCCGT	W63	
AC67	VCCGT	W64	
AC68	VCCGT	W65	
AC69	VCCGT	W66	
AC70	VCCGT	W67	
AC71	VCCGT	W68	
J43	VCCGT	W69	
J45	VCCGT	W70	
J46	VCCGT	W71	
J48	VCCGT	Y62	
J50	VCCGT		
J52	VCCGT		
J53	VCCGT		
J55	VCCGT	VCCGT_X_AK42	AK42
J56	VCCGT	VCCGT_X_AK43	AK43
J58	VCCGT	VCCGT_X_AK45	AK45
J60	VCCGT	VCCGT_X_AK46	AK46
K48	VCCGT	VCCGT_X_AK48	AK48
K50	VCCGT	VCCGT_X_AK50	AK50
K52	VCCGT	VCCGT_X_AK52	AK52
K53	VCCGT	VCCGT_X_AK53	AK53
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L64	VCCGT	VCCGT_X_AL46	AL46
L65	VCCGT	VCCGT_X_AL50	AL50
L66	VCCGT	VCCGT_X_AL53	AL53
L67	VCCGT	VCCGT_X_AL56	AL56
L68	VCCGT	VCCGT_X_AL58	AL58
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N66	VCCGT	VCCGT_X_AJ58	AJ58
N67	VCCGT	VCCGT_X_AJ83	AJ83
N69	VCCGT	VCCGT_X_BB57	BB57
		VCCGT_X_BB66	BB66



+VCC\_GTUS Reserve for soldering

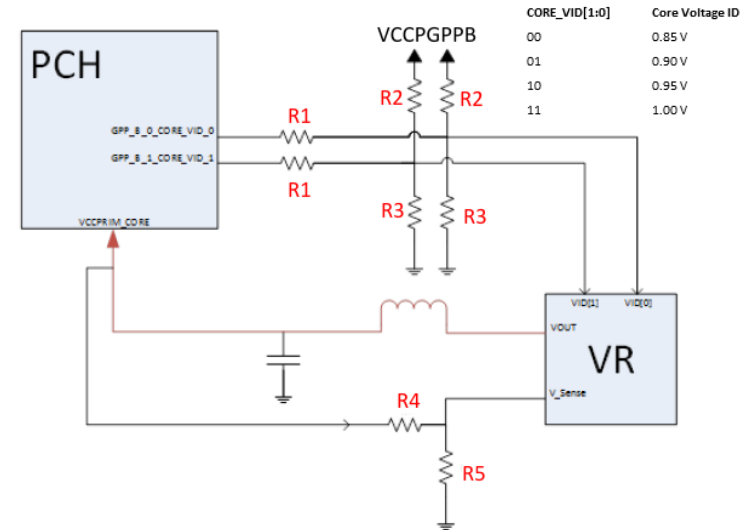
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Note1: VCCPRIM\_CORE Implementation with PCH CORE\_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



For Pre-ES Parts: Disconnect PCH CORE\_VID[1:0] to the VR and fix PCH VCCPRIM\_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM\_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE\_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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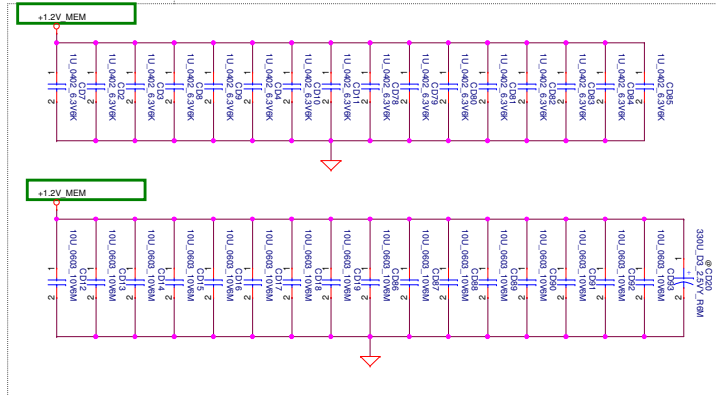
Title			CPU (14/14)	
Size	Document Number		Rev	
	LA-C621P		1.0	
Date:	Thursday, September 24, 2015	Sheet	19	of 60

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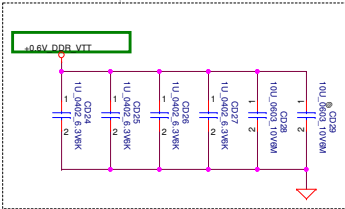
# JDIMM1 REV Type H=4

<7> DDR\_A\_DQS# [0..7] <<>>  
 <7> DDR\_A\_DQ [0..63] <<>>  
 <7> DDR\_A\_DQS# [0..7] <<>>  
 <7> DDR\_A\_MA [0..16] <<>>

Layout Note:  
Place near JDIMM1

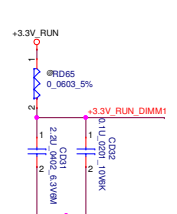
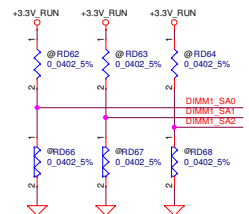


Layout Note:  
Place near  
JDIMM1.203,204



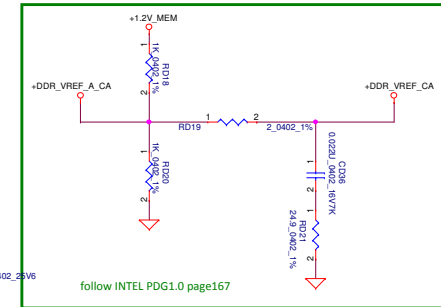
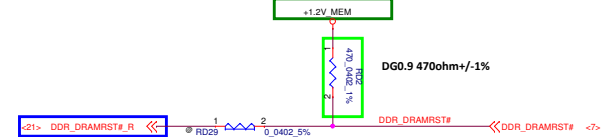
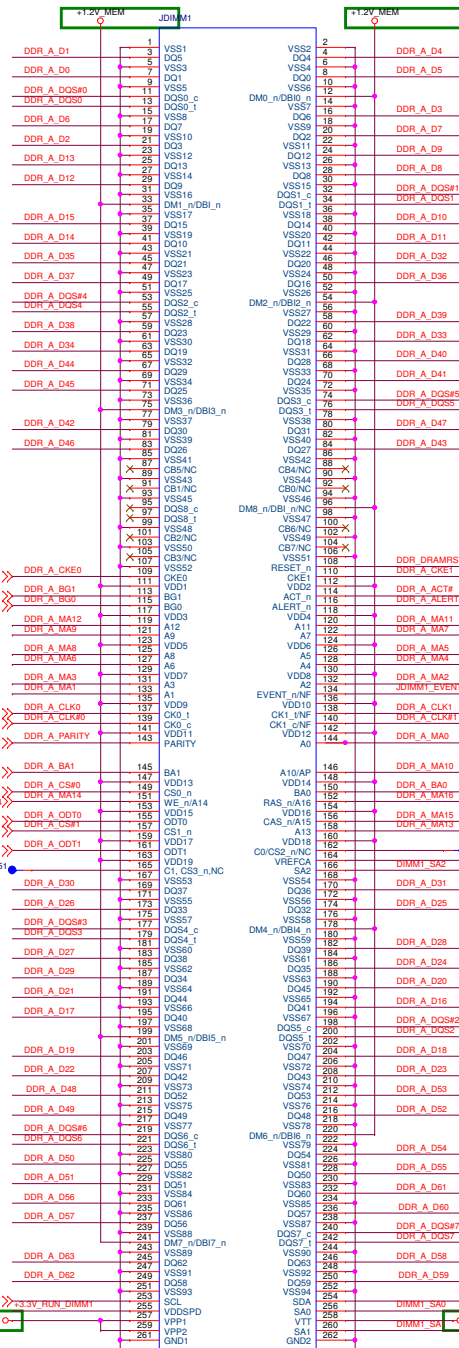
## DIMM Select

	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0

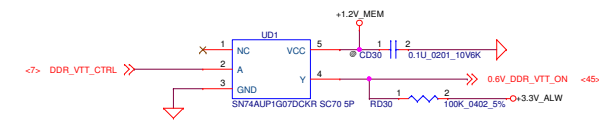


<8,14,21,42> DDR\_XDP\_WAN\_SMBCLK <<>> <3.3V RUN DIMM1>

<2.5V MEM>



follow INTEL PDG1.0 page167



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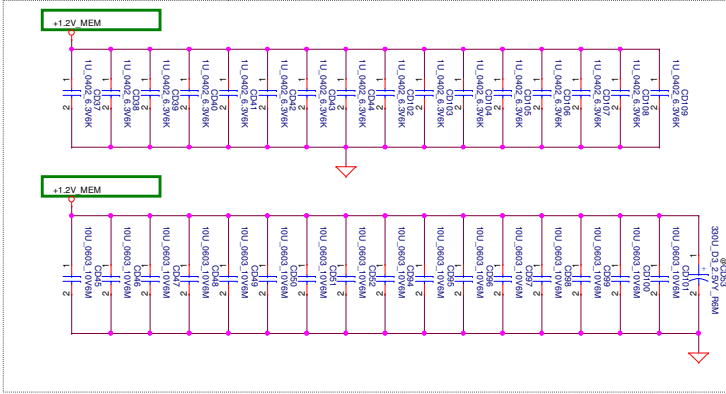


File	DDR4
Size	Document Number
Date	Thursday, September 24, 2015
Sheet	20 of 60

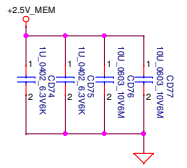
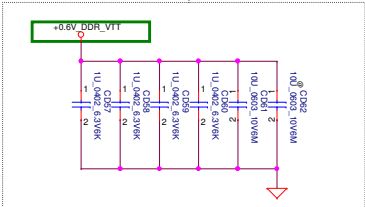
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<-> DDR\_B\_DQS[0..7] <<>>  
 <-> DDR\_B\_D[0..63] <<>>  
 <-> DDR\_B\_DQS[0..7] <<>>  
 <-> DDR\_B\_MA[0..16] <<>>

Layout Note:  
Place near JDIMM2

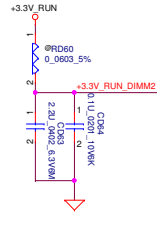
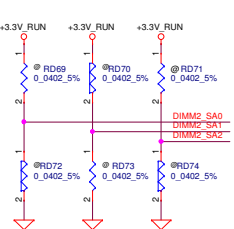


Layout Note:  
Place near  
JDIMM2\_203,204



## DIMM Select

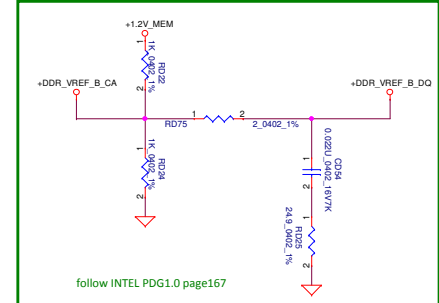
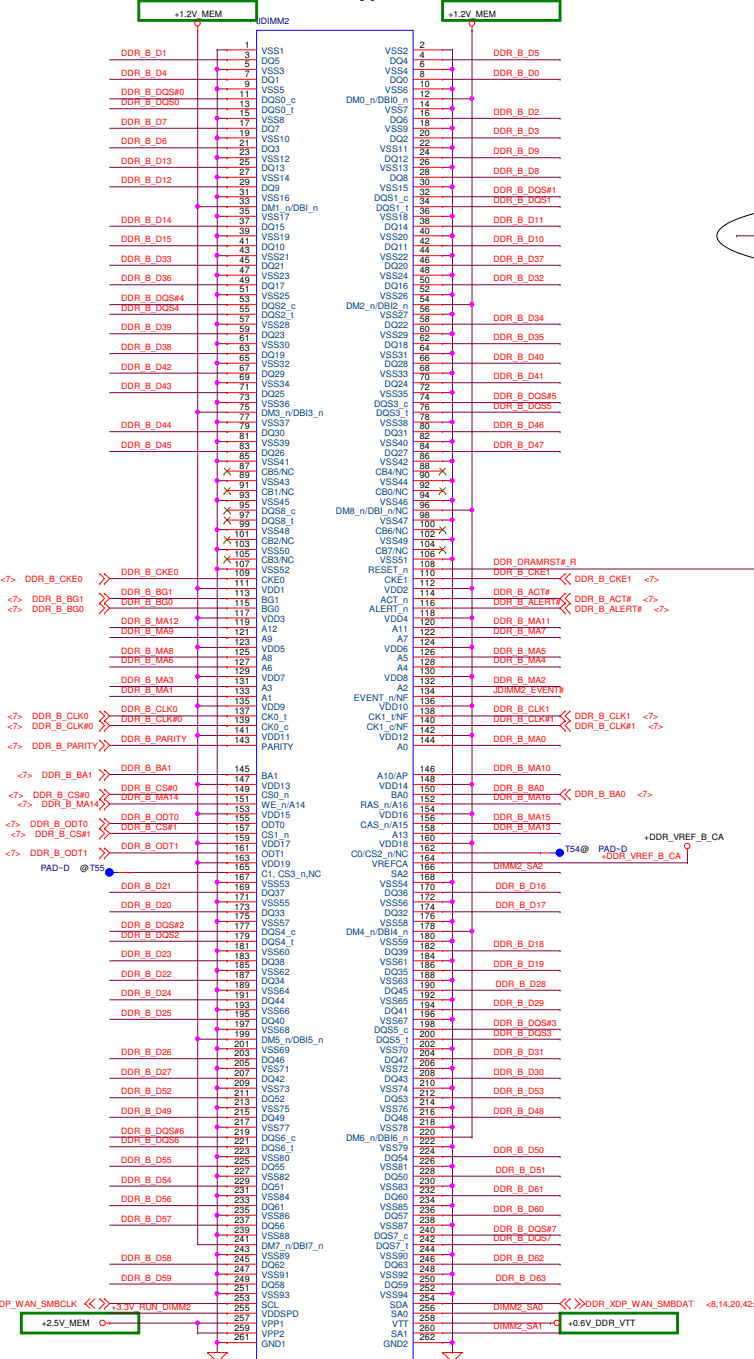
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



<-> B.14,0.42<-> DDR\_XDP\_WAN\_SMBCLK <<>>

+2.5V\_MEM

## JDIMM2 REV Type H=4



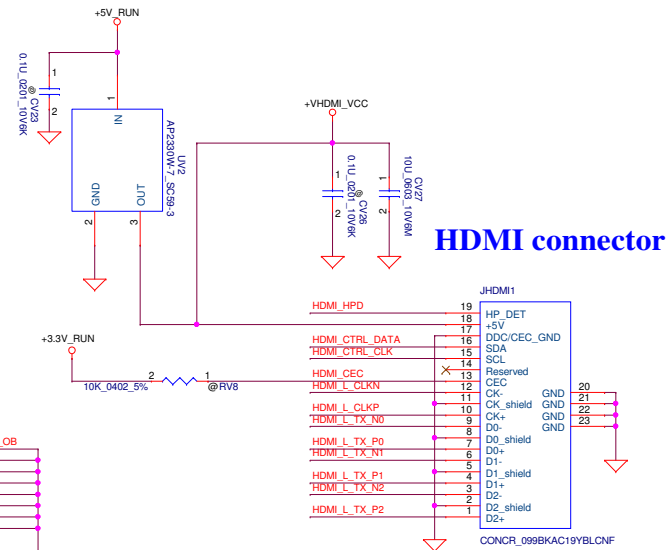
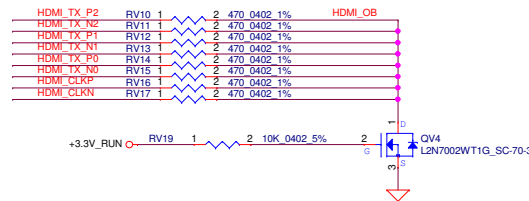
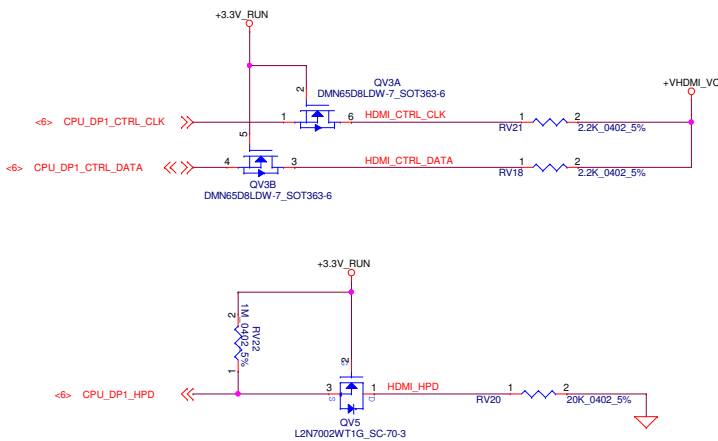
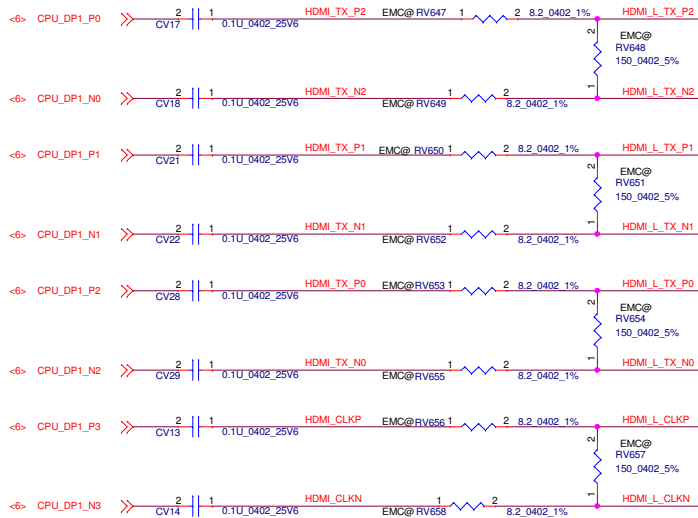
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of	60

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HDMI CONN

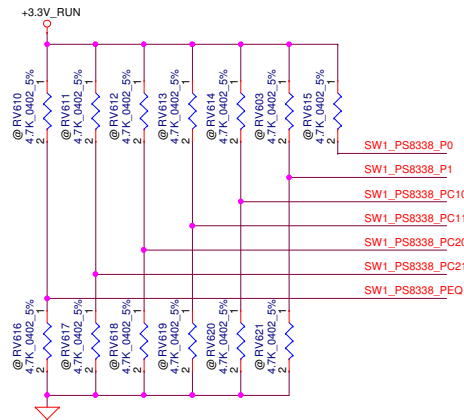
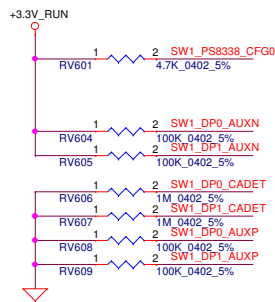
LA-C621P

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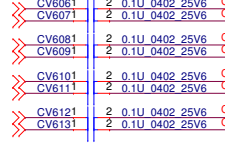


Title		Rev	
HDMI CONN		1.0	
Size	Document Number	Date	Sheet
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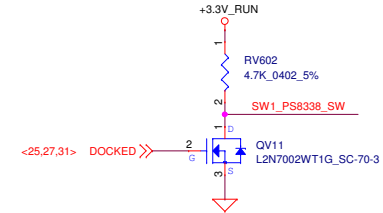
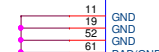
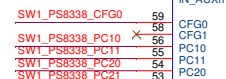
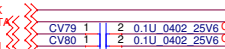
<6> CPU\_DP2\_P0  
CPU\_DP2\_N0  
<6> CPU\_DP2\_P1  
CPU\_DP2\_N1  
<6> CPU\_DP2\_P2  
CPU\_DP2\_N2  
<6> CPU\_DP2\_P3  
CPU\_DP2\_N3



<6> CPU\_DP2\_HP0  
SW1\_PS8338\_P1  
SW1\_PS8338\_P0

for support TMDS signal need contact SCL/SDA to P22,23

<6> CPU\_DP2\_CTRL\_CLK  
<6> CPU\_DP2\_CTRL\_DATA  
<6> CPU\_DP2\_AUXP  
<6> CPU\_DP2\_AUXN



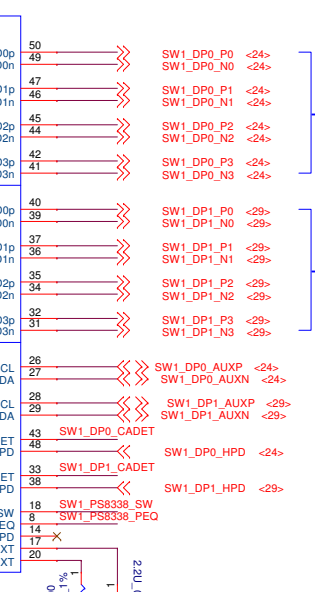
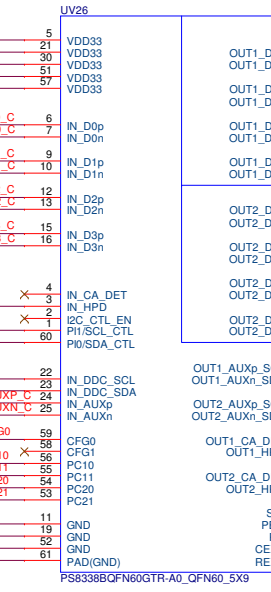
<25,27,31> DOCKED

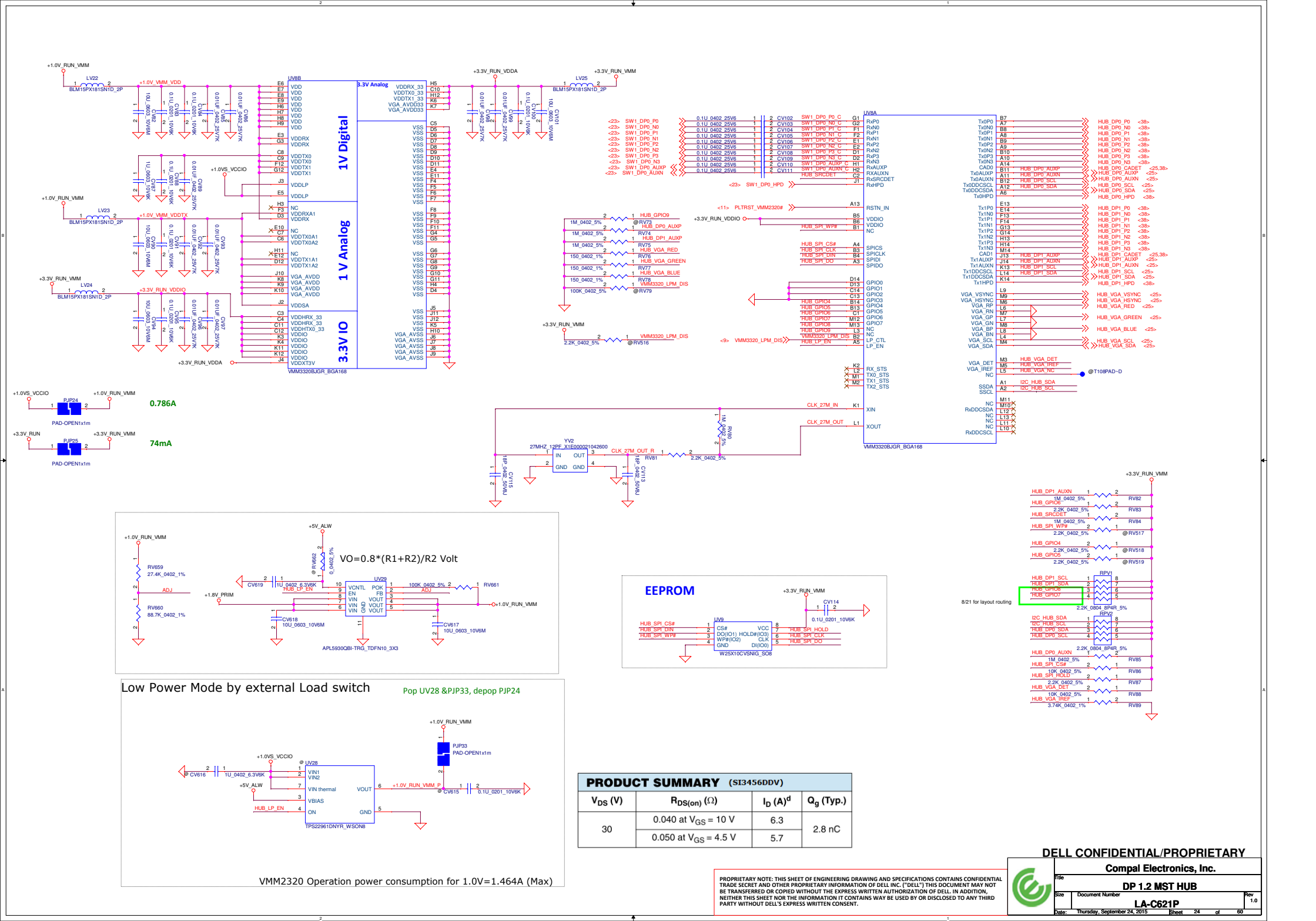
Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O

For Control Switching Mode (CFG0 = L):  
SW = L: Port1 is selected (default)  
SW = H: Port2 is selected

For Automatic Switching Mode (CFG0 = H):  
SW = L: Port1 has higher priority when both ports are plugged (default)  
SW = H: Port2 has higher priority when both ports are plugged

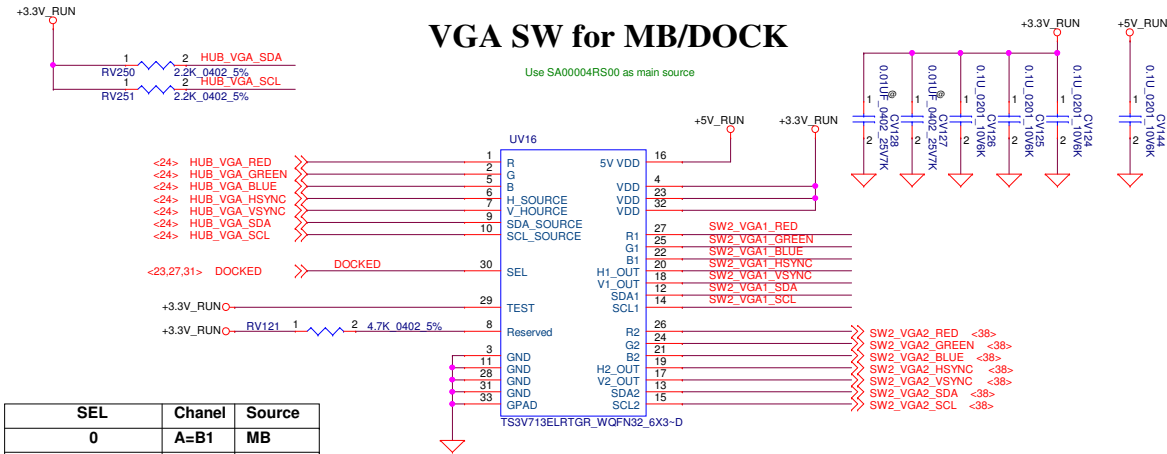
Dock has high priority when both ports plugged



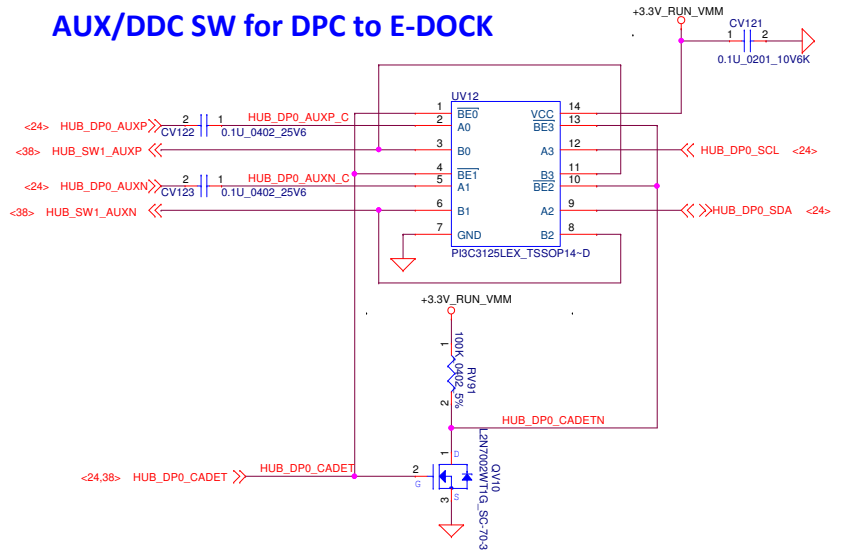


## VGA SW for MB/DOCK

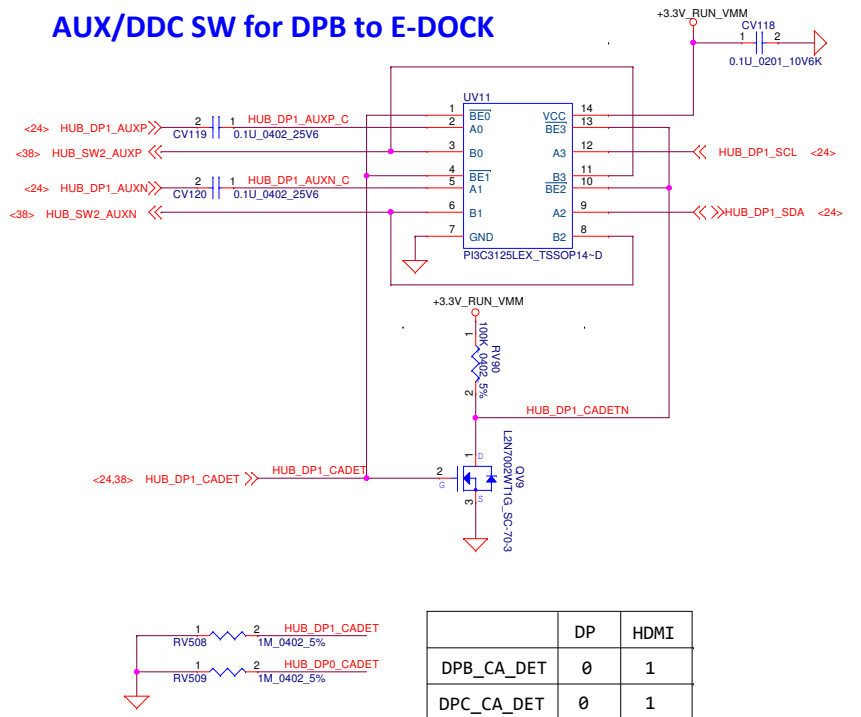
Use SA00004RS00 as main source



## AUX/DDC SW for DPC to E-DOCK



## AUX/DDC SW for DPB to E-DOCK

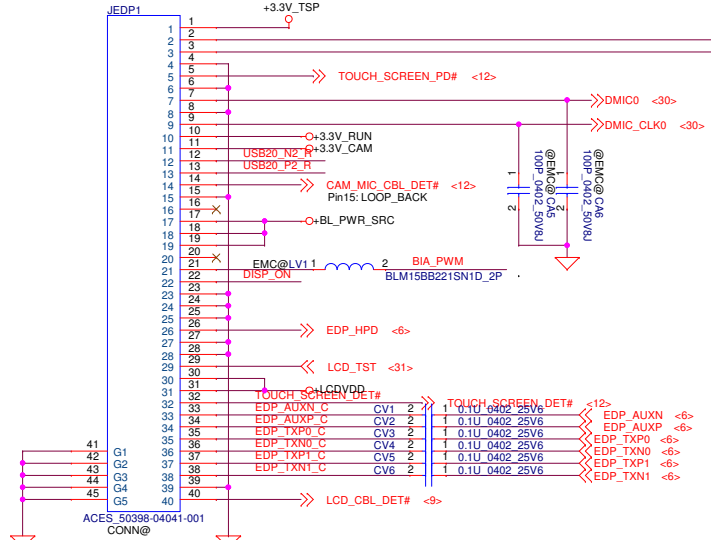


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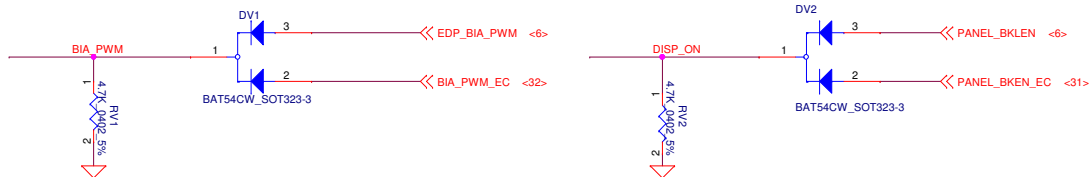
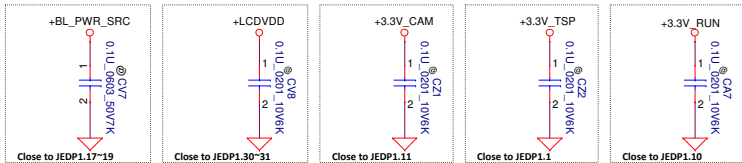
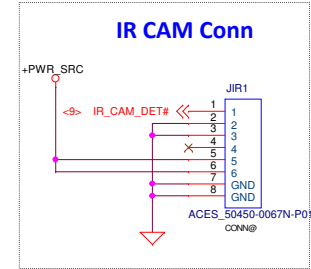
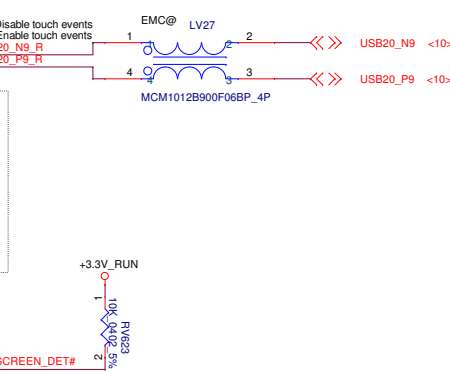
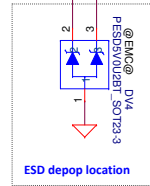
Compal Electronics, Inc.			
Title			
DP SW			
Size	Document Number	Rev 1.0	
Date: Thursday, September 24, 2015		Sheet 25	of 60

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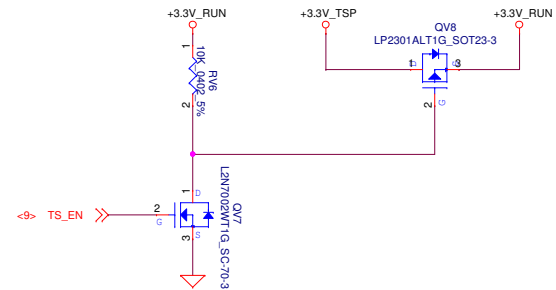
# LINK 50398-04041-001 DONE



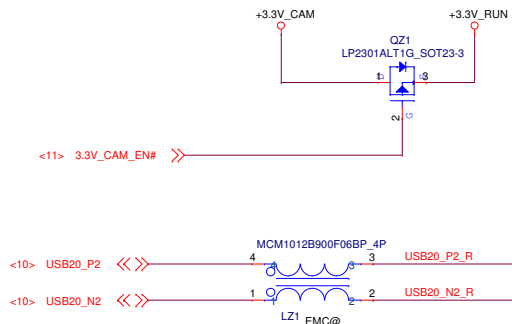
TOUCH\_PANEL\_INTR#:  
Close lid >> TP\_EN = 0 >> Disable touch events  
Open lid >> TP\_EN = 1 >> Enable touch events



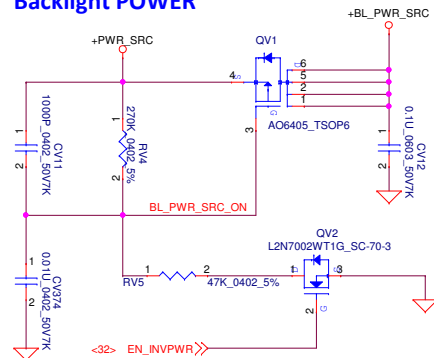
## For Touchscreen



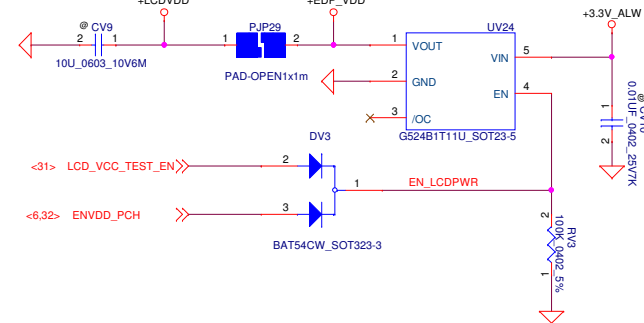
## WebCAM



## Backlight POWER



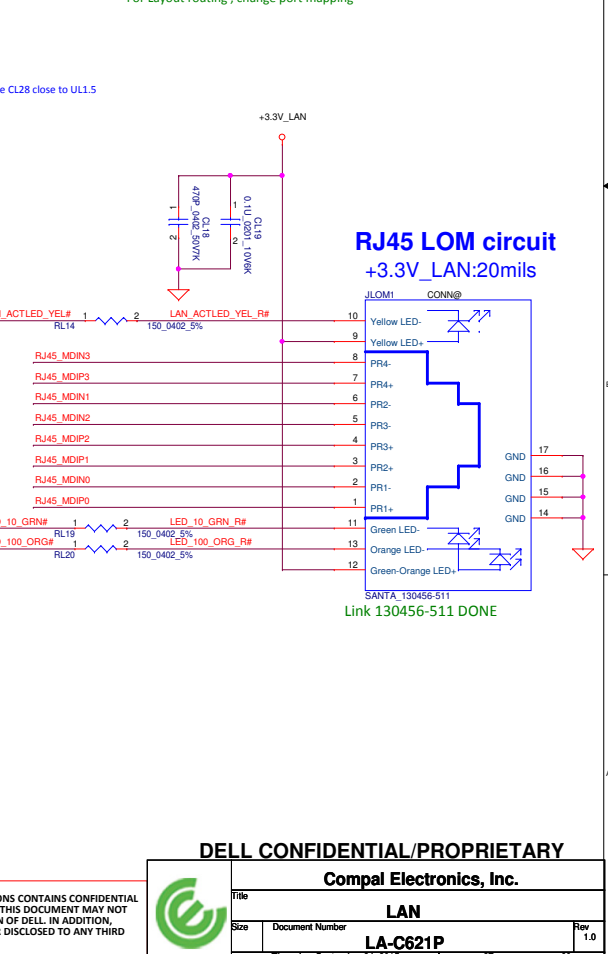
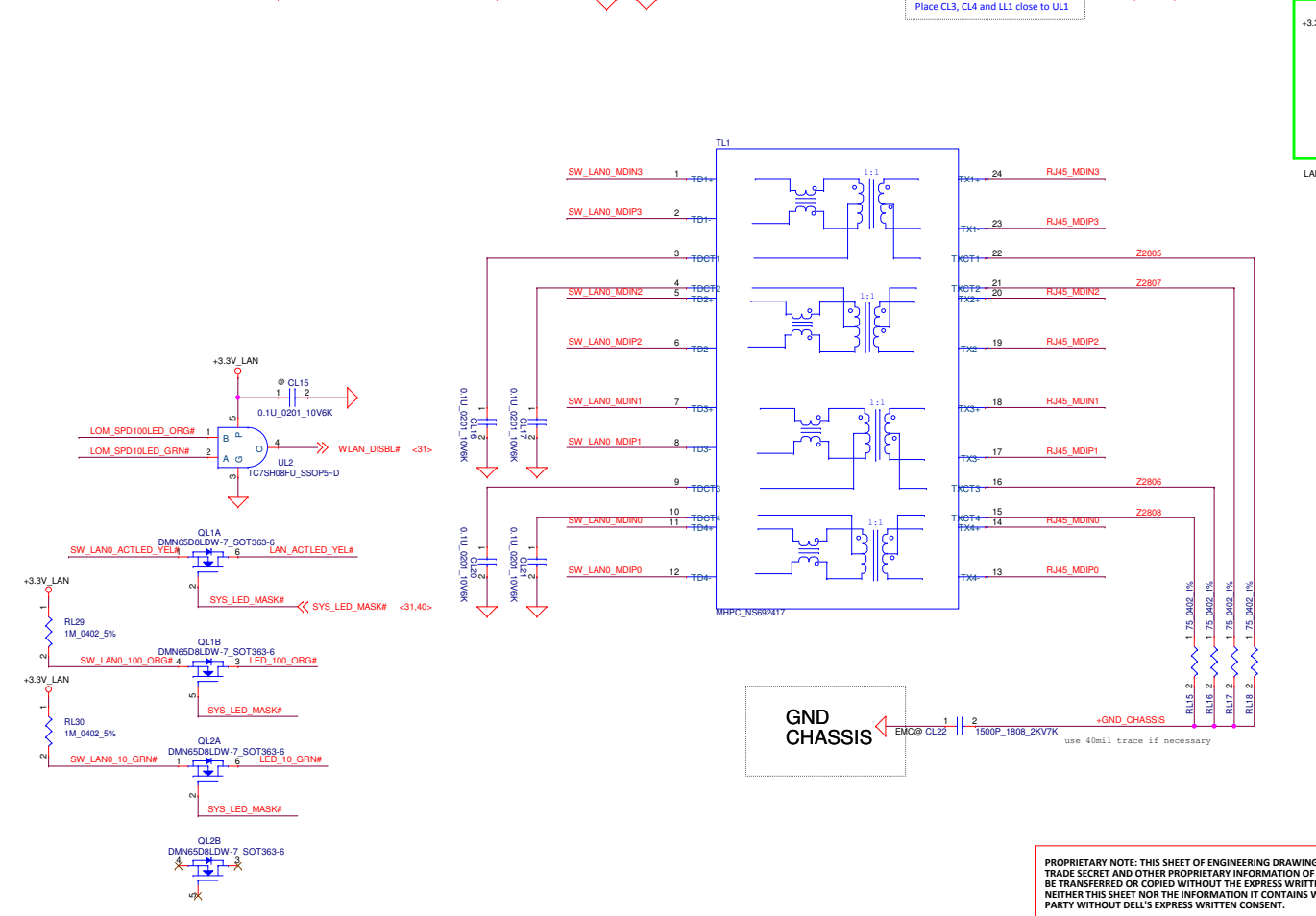
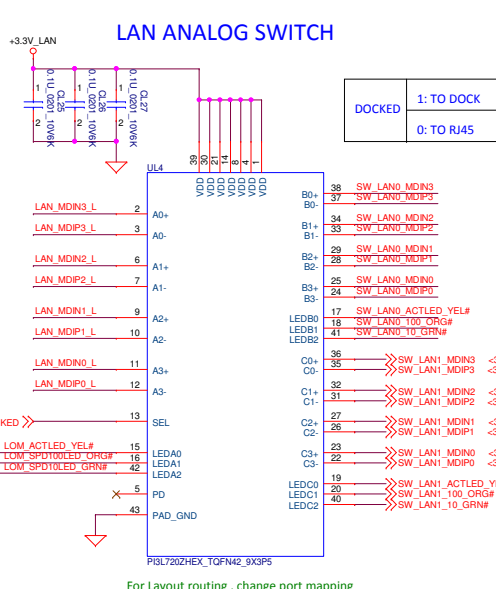
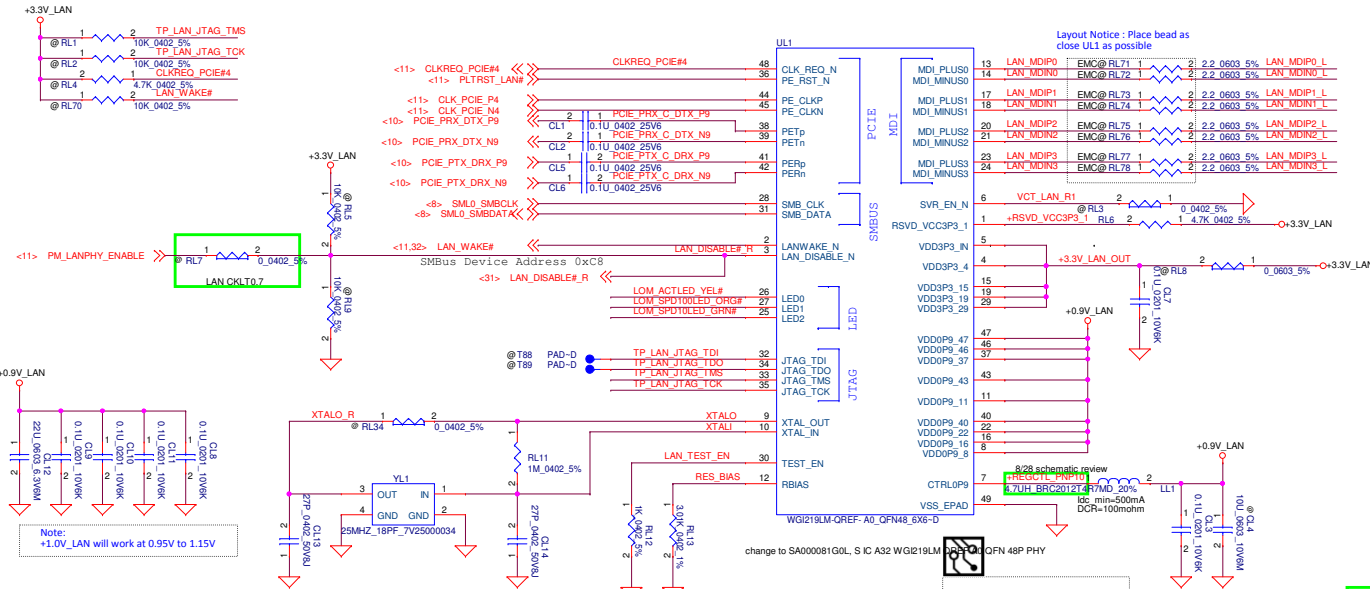
## LCDVDD POWER



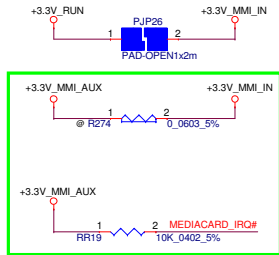
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eDP CONN & Touch screen			
Size	Document Number	Rev	
		1.0	
Date:	Thursday, September 24, 2015	Sheet	26 of 60

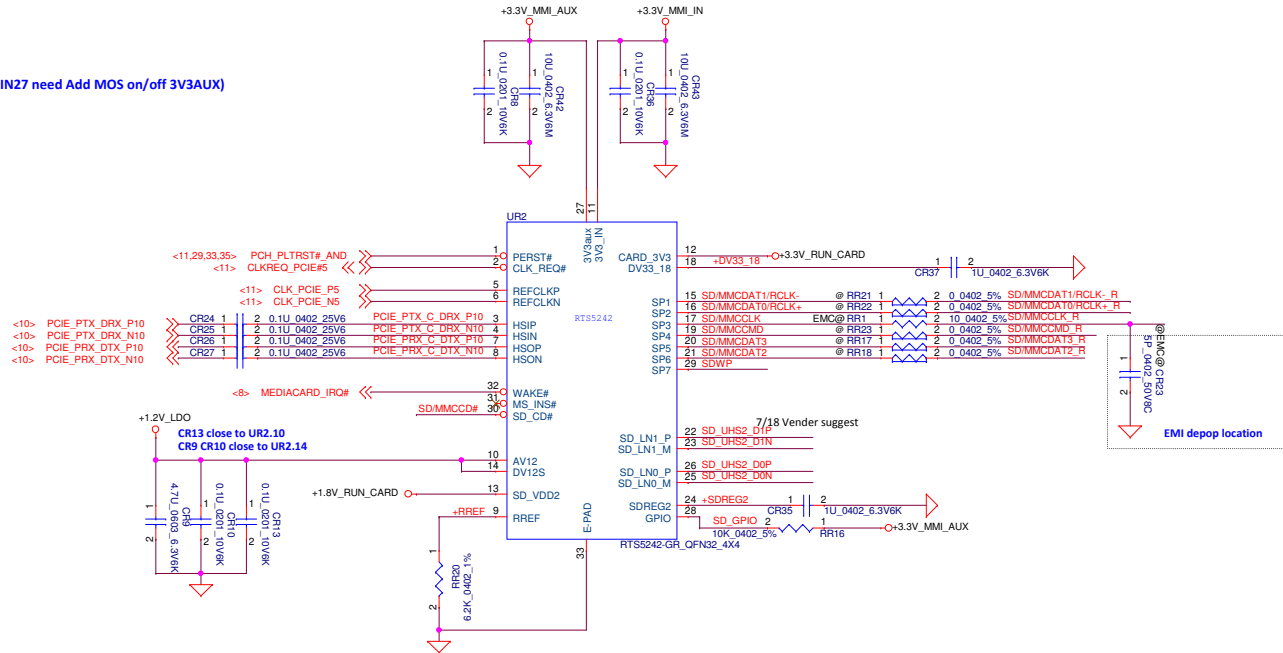


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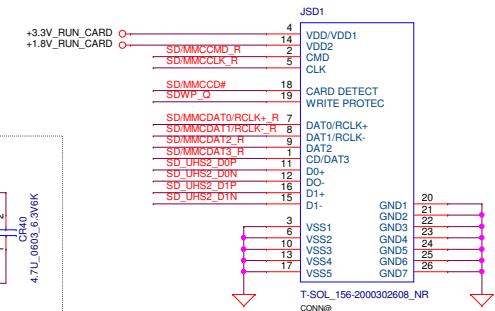
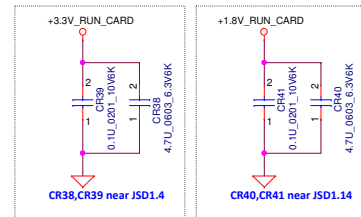
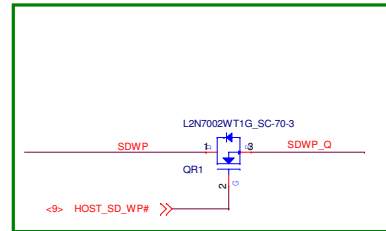


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)



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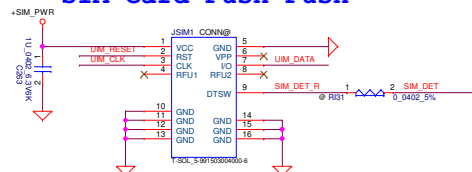
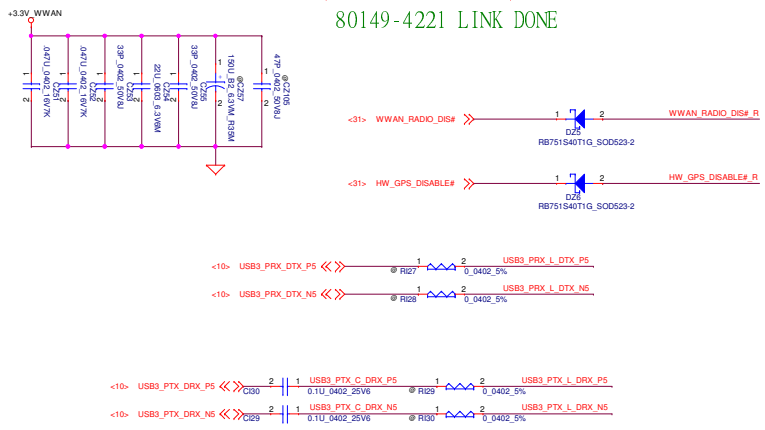
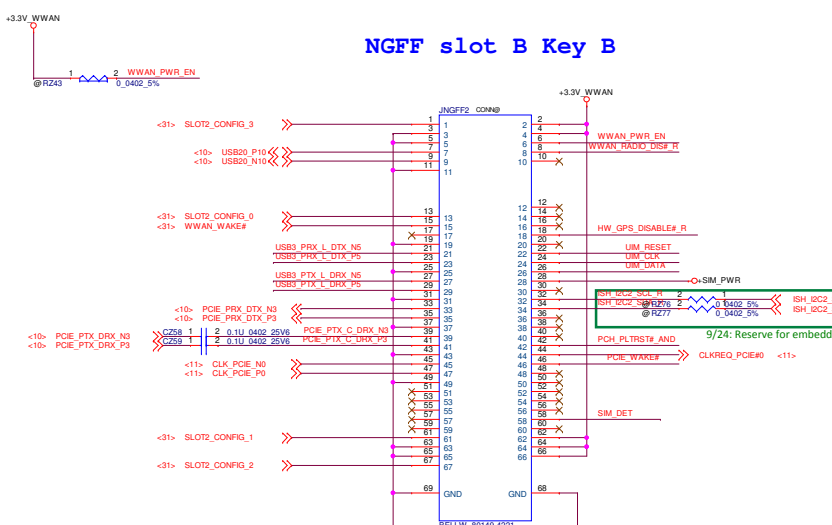
Compal Electronics, Inc.

Card Reader

LA-C621P

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[illegible][illegible]

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				



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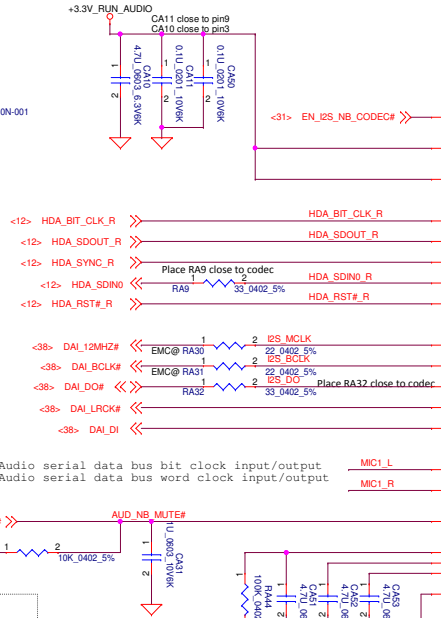
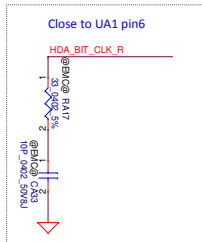
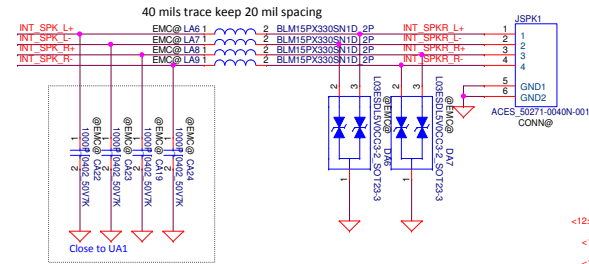
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Size	Document Number	LA-C621P	
Date:	Thursday, September 24, 2015	Sheet	29 of 60



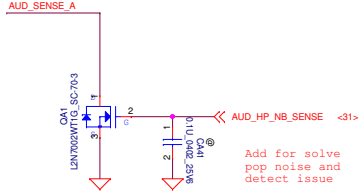
1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box.)

## Internal Speakers Header

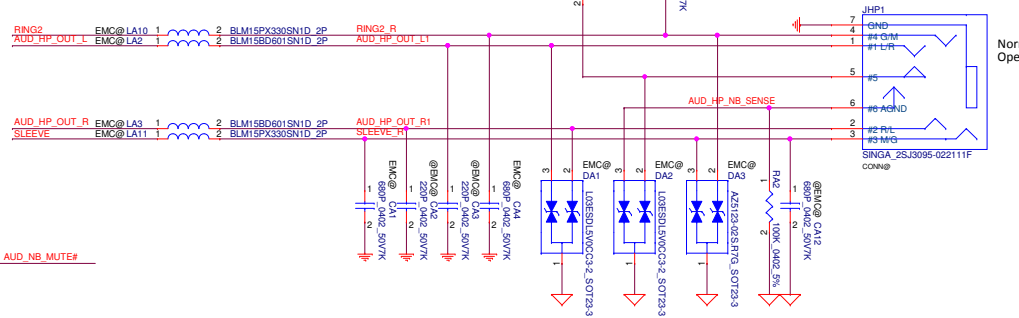
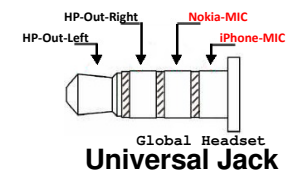
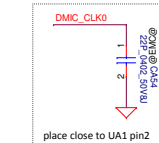
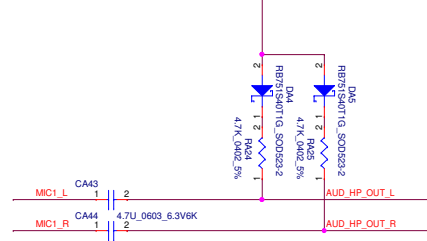
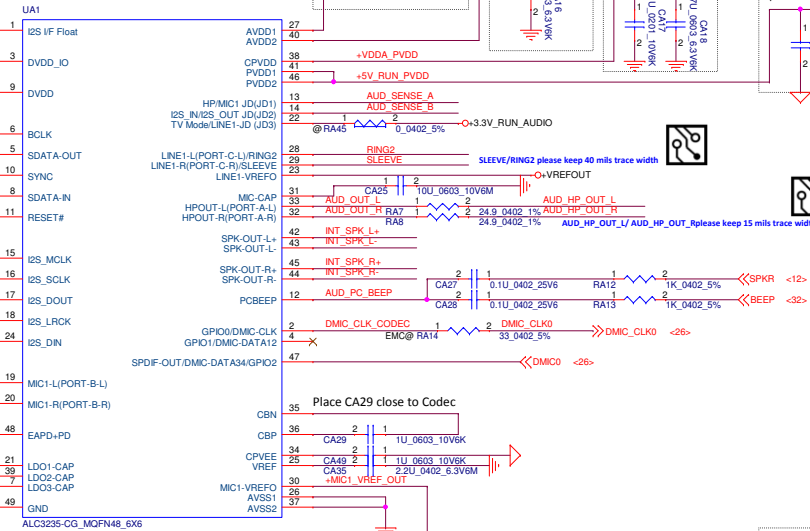
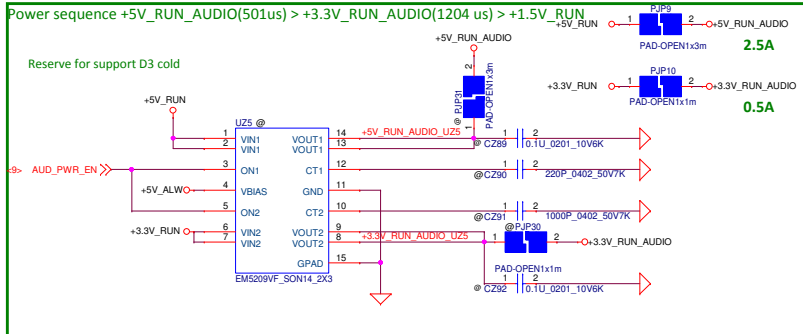
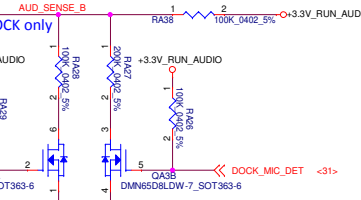
40 mils trace keep 20 mil spacing



Place closely to Pin 13.



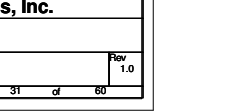
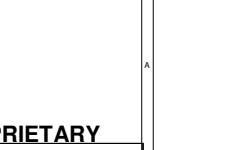
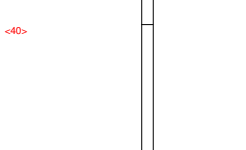
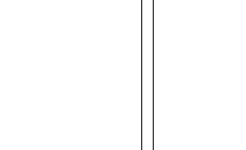
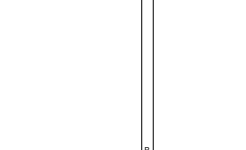
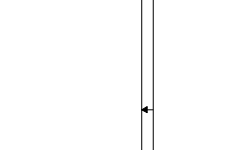
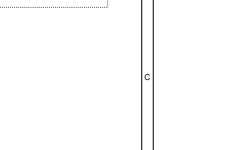
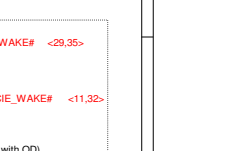
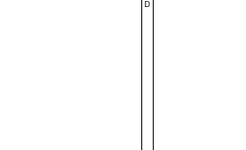
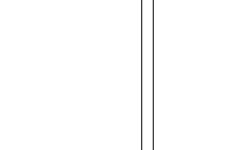
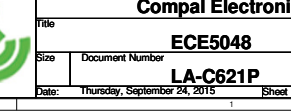
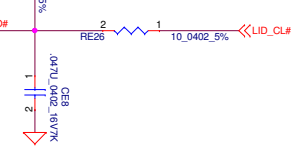
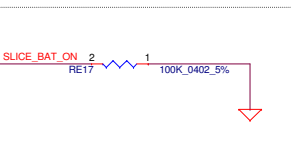
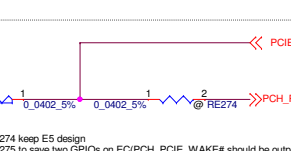
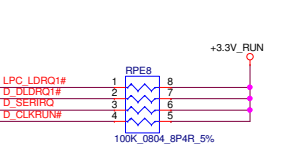
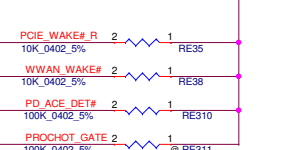
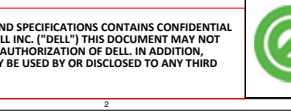
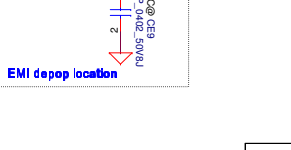
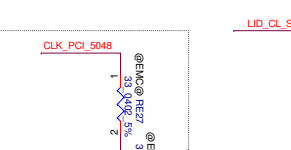
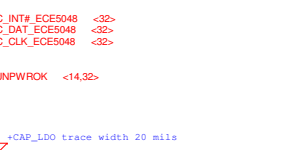
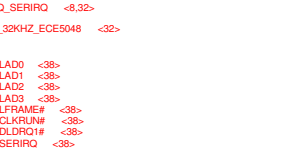
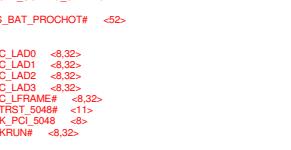
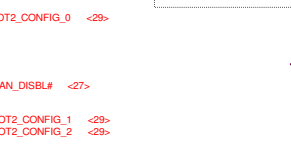
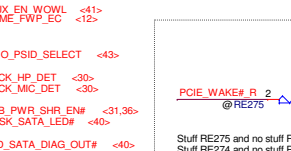
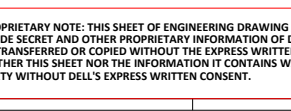
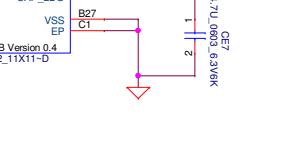
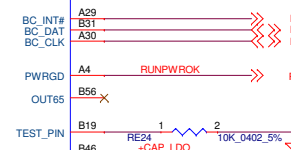
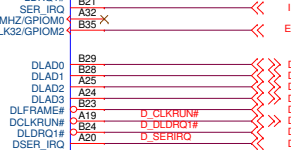
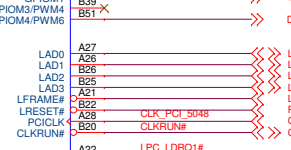
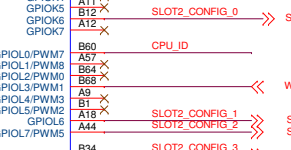
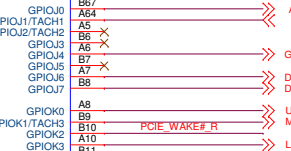
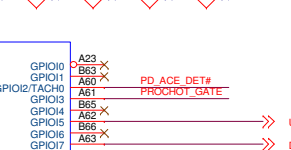
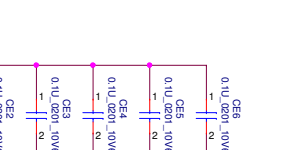
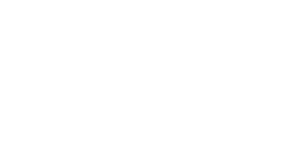
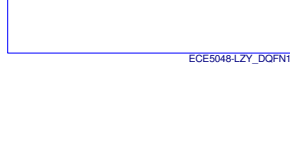
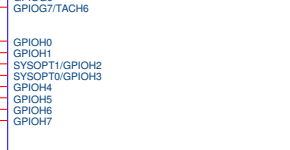
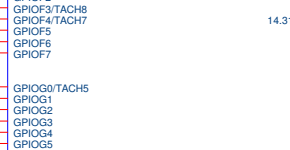
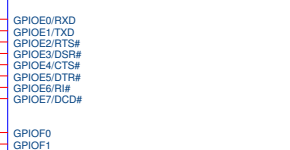
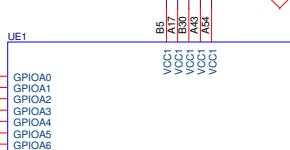
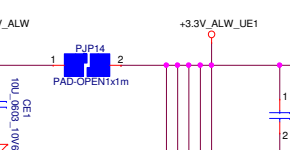
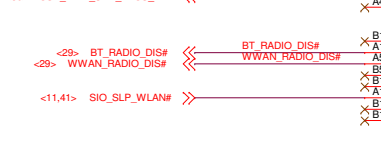
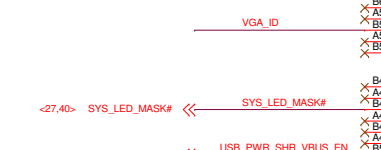
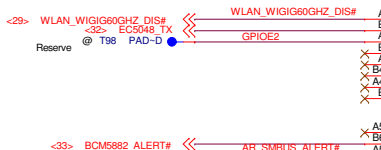
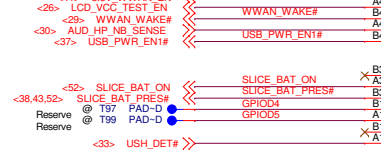
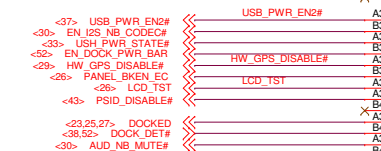
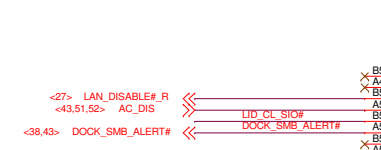
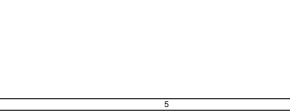
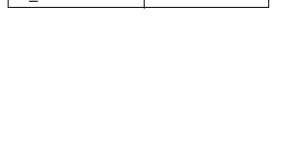
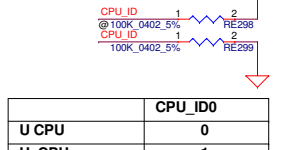
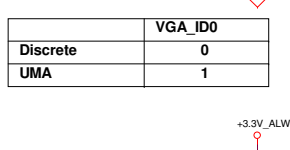
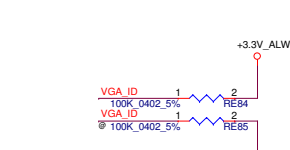
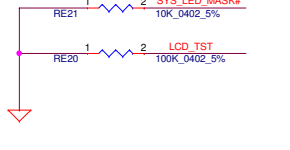
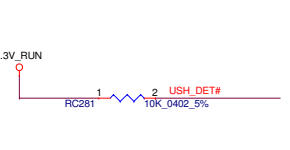
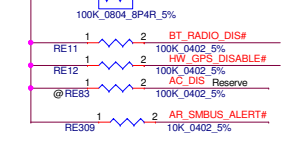
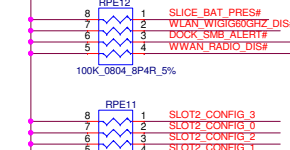
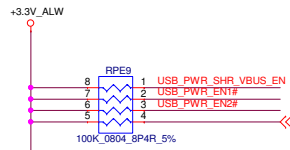
Place closely to Pin 14 for DOCK only



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Codex ALC3235	
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	VGA_ID0
Discrete	0
UMA	1

	CPU_ID0
U_CPU	0
H_CPU	1

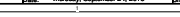
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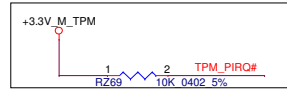
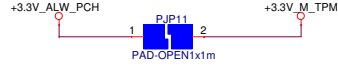
Compal Electronics, Inc.



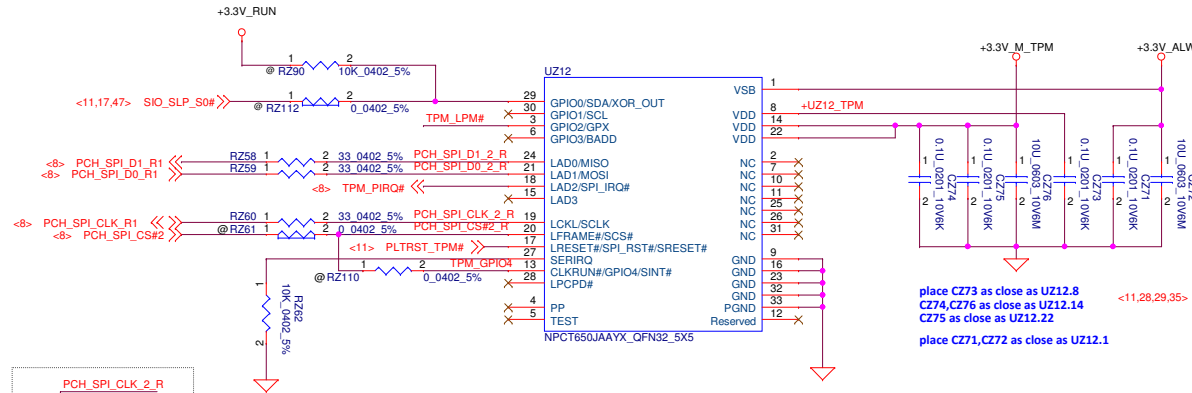
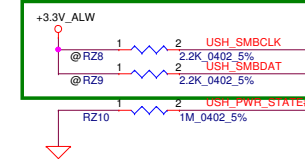
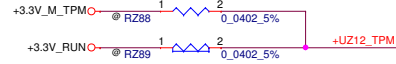
ECE5048		Rev 1.0
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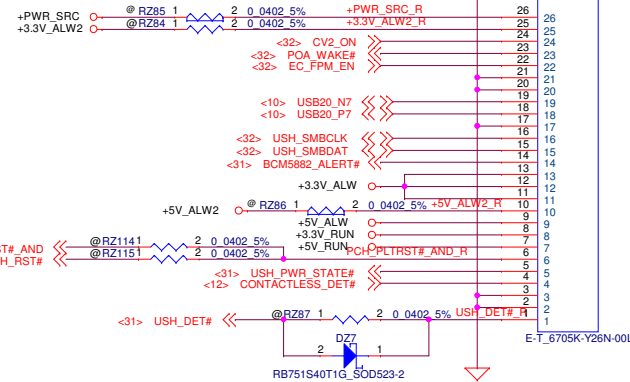
power rail option: TPM power rail must same as +3.3V\_SPI (SPI ROM)



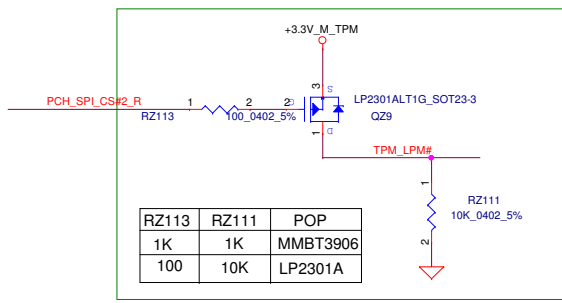
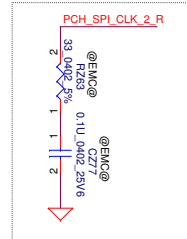
7/18 vnder suggest.



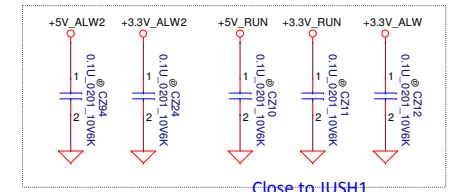
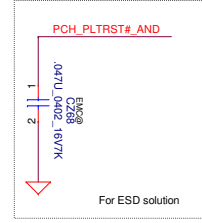
place CZ73 as close as UZ12.8  
CZ74,CZ76 as close as UZ12.14  
CZ75 as close as UZ12.22  
place CZ71,CZ72 as close as UZ12.1



## USH CONN



RZ113	RZ111	POP
1K	1K	MMBT3906
100	10K	LP2301A



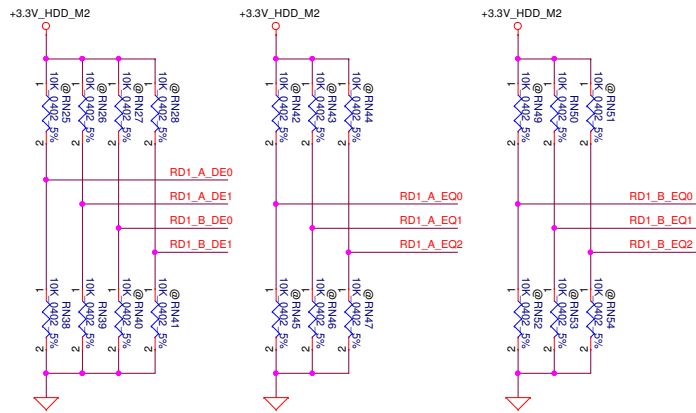
Close to JUSH1

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Title		
USH & TPM		
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Programmable output de-emphasis level setting for channel A.  
A\_DE0: internally pulled up at ~150K;  
A\_DE1 internally pulled down at ~150K

[A\_DE1,A\_DE0] ==  
LL: -7.5dB  
HL: -2dB  
LH: -3.5dB (default)  
HH: -6dB

Programmable output de-emphasis level setting for channel B.  
B\_DE0: internally pulled up at ~150K;  
B\_DE1 internally pulled down at ~150K

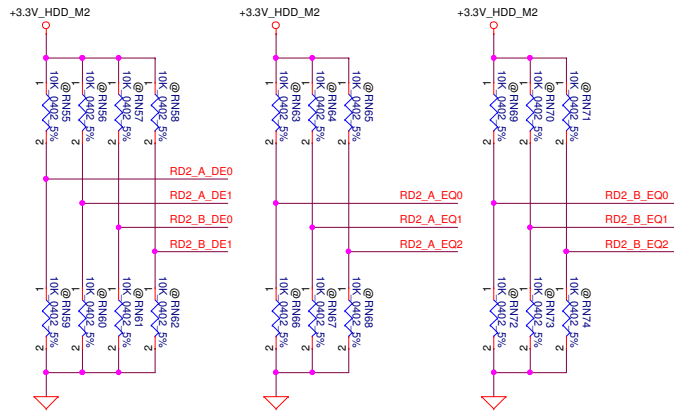
[B\_DE1,B\_DE0] ==  
LL: -7.5dB  
HL: -2dB  
LH: -3.5dB (default)  
HH: -6dB

Equalizer control and program for channel A.  
A\_EQ0, A\_EQ1 and A\_EQ2: internally pulled down at ~150K

[A\_EQ2,A\_EQ1,A\_EQ0] ==  
LLL: EQ Level1(default)  
LHL: EQ Level2  
LHL: EQ Level3  
HLL: EQ Level4  
LHL: EQ Level5  
LHH: EQ Level6  
LHL: EQ Level7  
HHH: EQ Level8

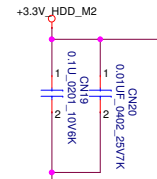
Equalizer control and program for channel B.  
B\_EQ0, B\_EQ1 and B\_EQ2: internally pulled down at ~150K

[B\_EQ2,B\_EQ1,B\_EQ0] ==  
LLL: EQ Level1(default)  
LHL: EQ Level2  
LHL: EQ Level3  
HLL: EQ Level4  
LHL: EQ Level5  
LHH: EQ Level6  
LHL: EQ Level7  
HHH: EQ Level8

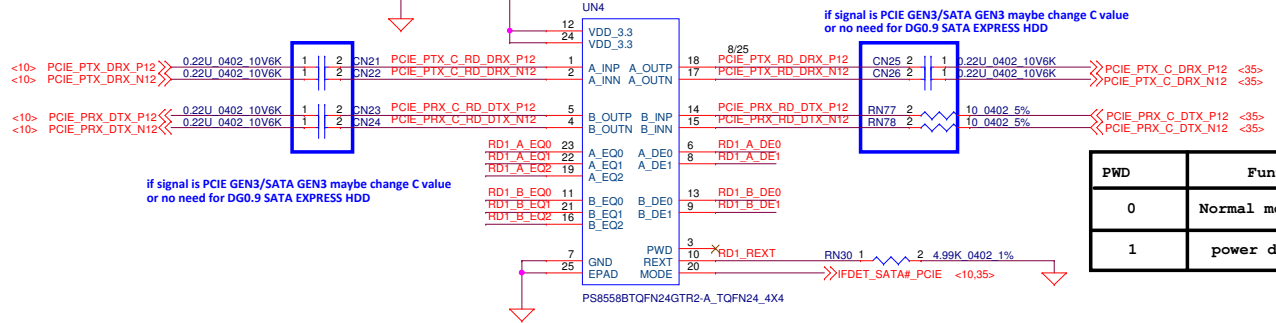


## SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>



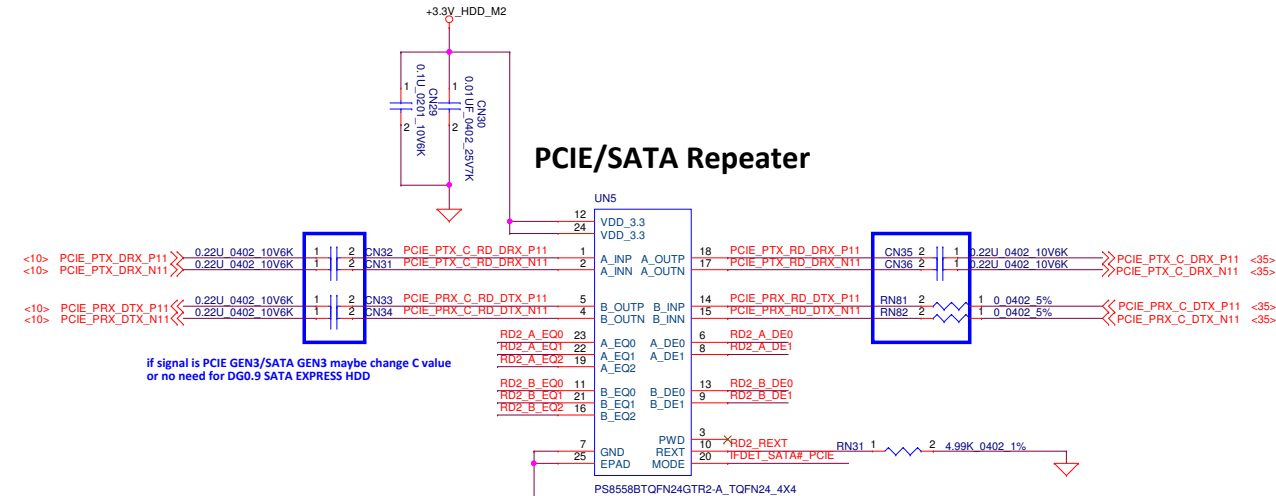
## PCIe/SATA Repeater



IFDET_SATA#_PCIE (SATA#PCIE0)	FLEX IO 11
0	PCIE
1	SATA

PWD	Funtion
0	Normal mode (default)
1	power down mode

## PCIe/SATA Repeater

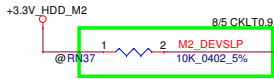
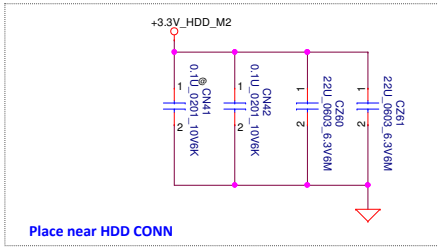


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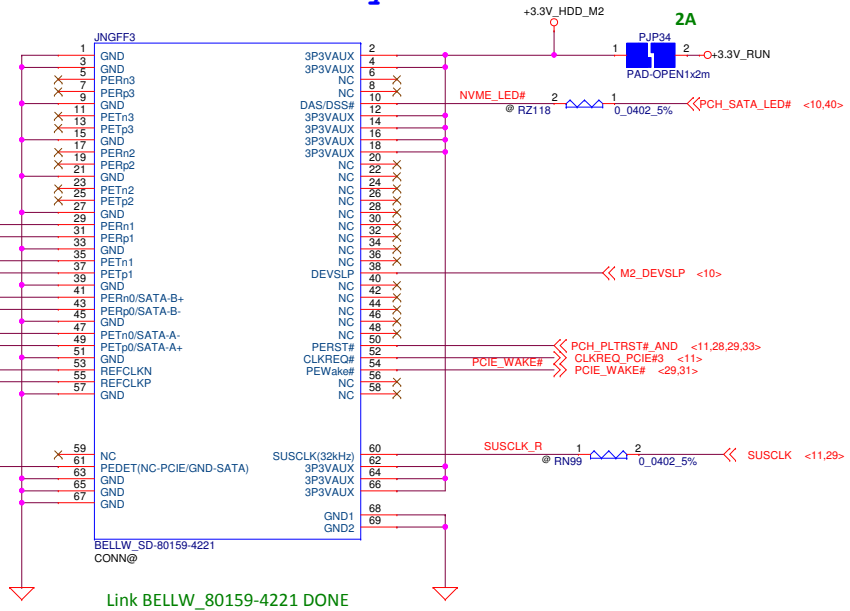


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Double check P/N

<10,34> IFDET\_SATA#\_PCIE

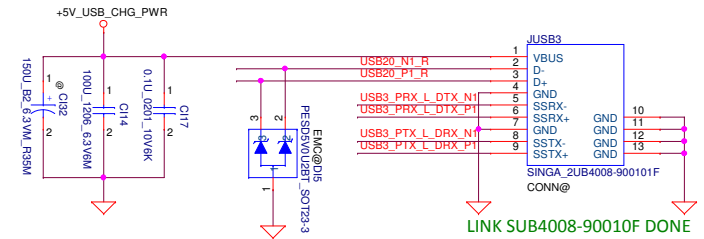
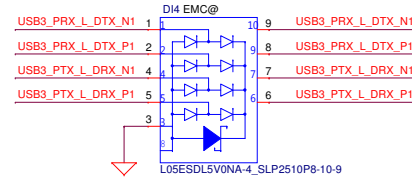
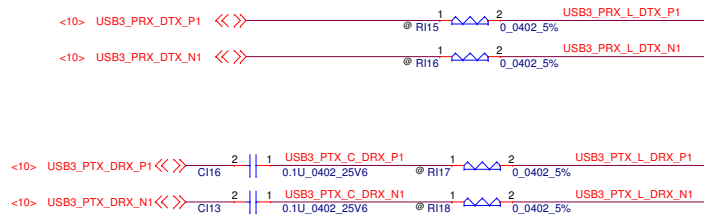
## 2280 SSD NGFF slot C Key M



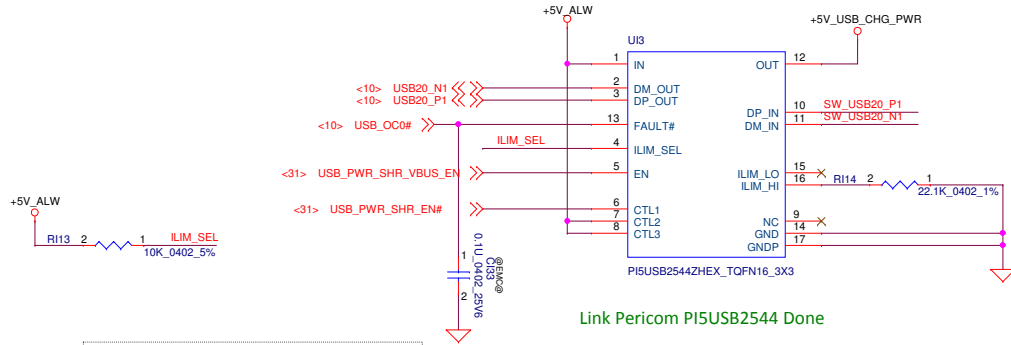
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Title HDD CONN			
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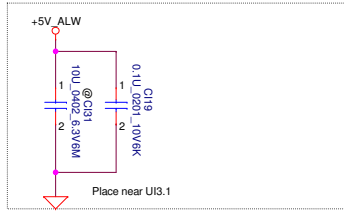
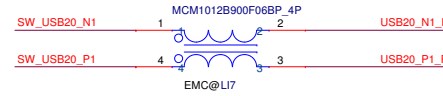
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LINK SUB4008-90010F DONE



Link Pericom PISUSB2544 Done



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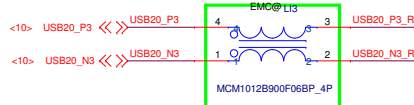
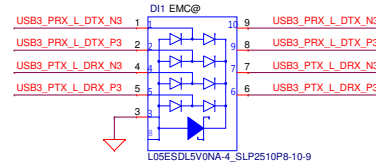
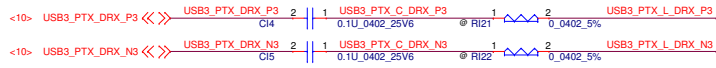
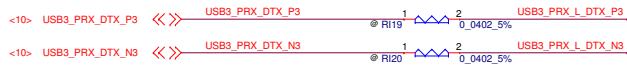
Compal Electronics, Inc.

USB SW

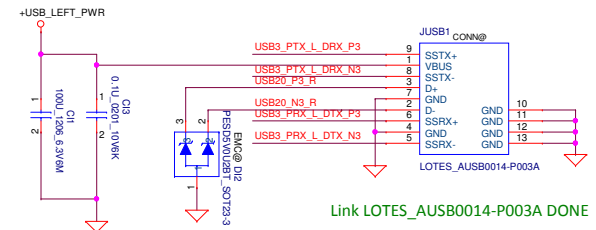
LA-C621P

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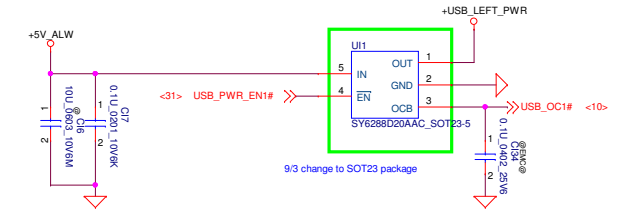




8/19 for layout routing change

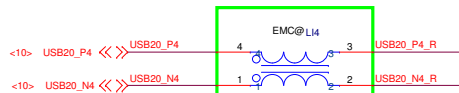
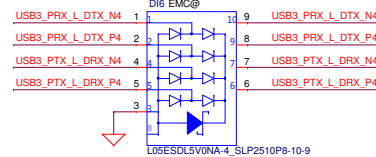
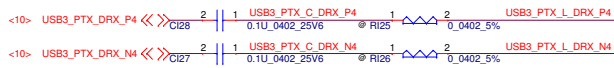


Link L05ESDL5V0NA-4\_SLP2510P8-10-9 DONE

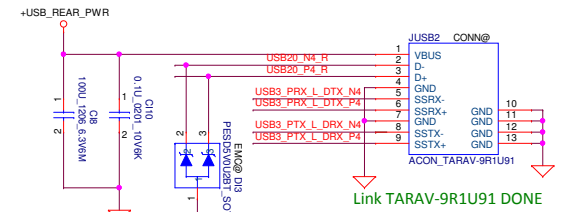


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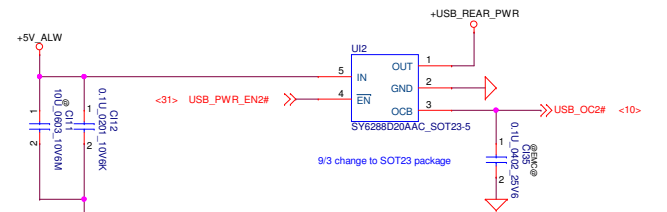
9/3 change to SOT23 package



8/19 for layout routing change



Link TARAV-9R1U91 DONE



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9/3 change to SOT23 package

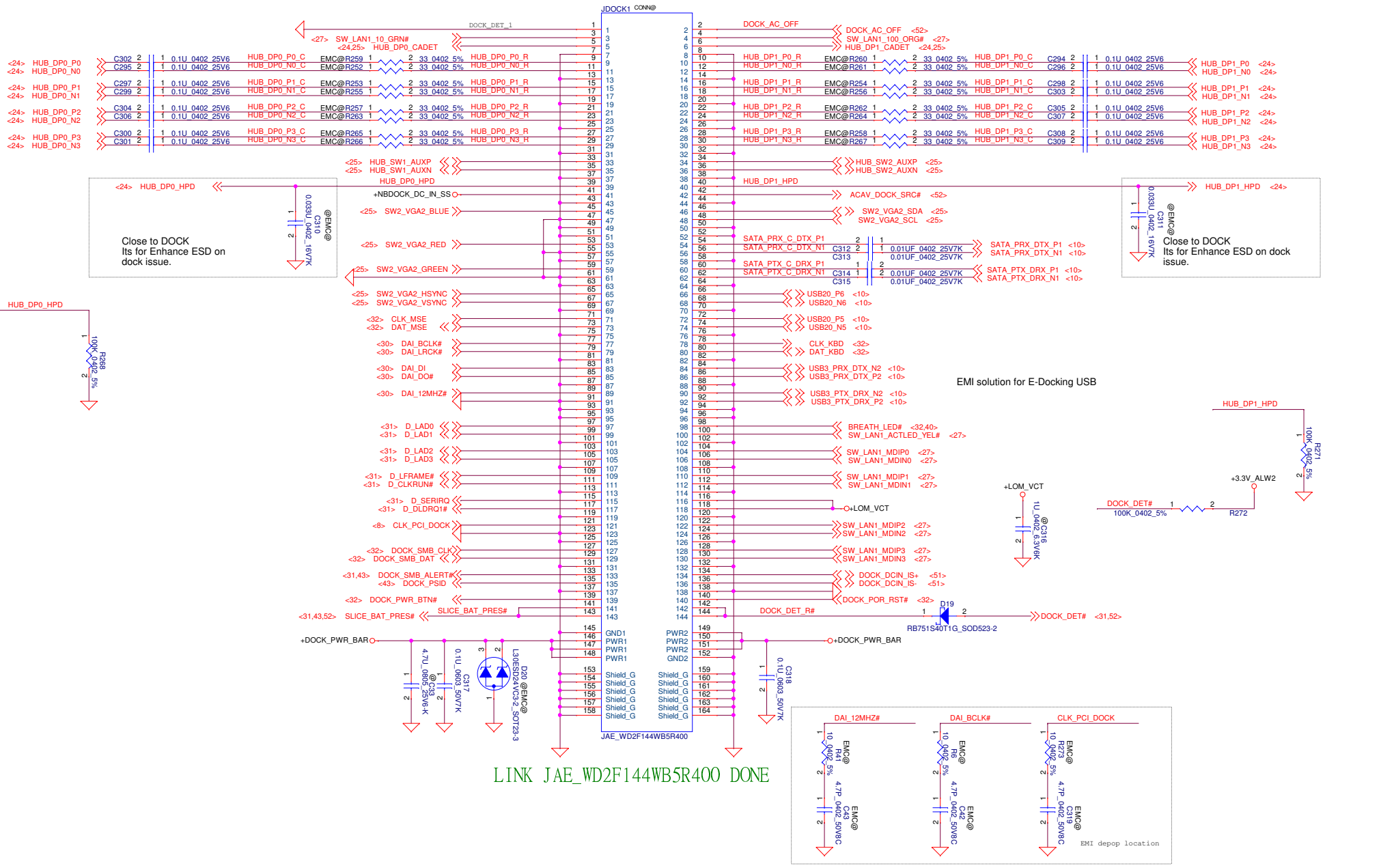
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Size	Document Number	LA-C621P	Rev 1.0
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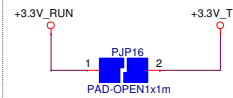
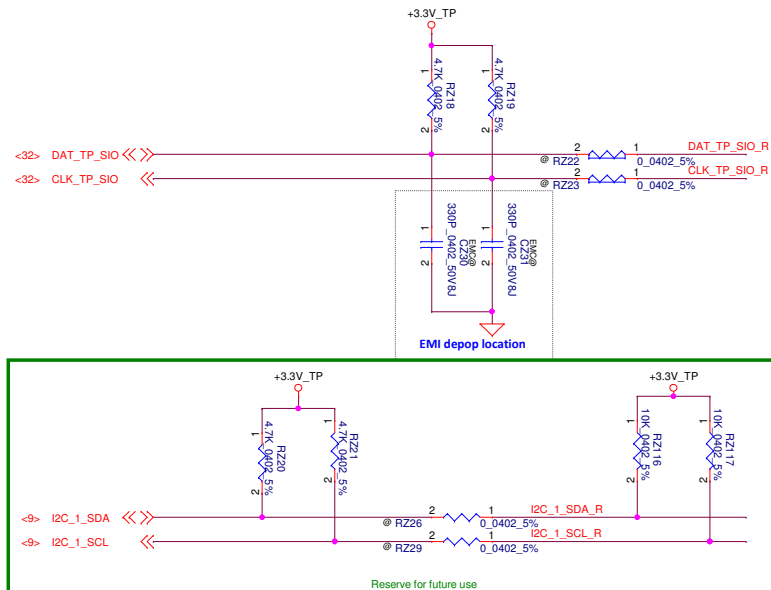
E-Dock

LA-C621P

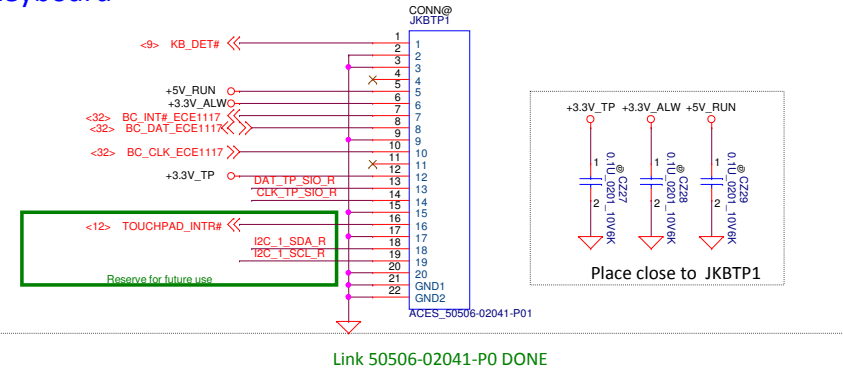
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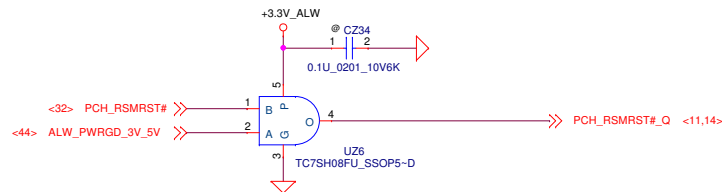
## Touch Pad



## Keyboard



## RSMRST circuit



### @eDP Cable W CAM

Part Number	Description
DC02C007600	H-CONN SET 13D MB-EDP-CAMERA

### @eDP TS Cable W CAM

Part Number	Description
DC02C007C00	H-CONN SET 13D MB-EDP-CAMERA-TS

### @eDP Cable W/O CAM

Part Number	Description
DC02C007D00	H-CONN SET 13D MB-EDP

### @SATA SPINDLE Cable

Part Number	Description
DC02C007500	H-CONN SET 13D MB-SPINDLE HDD

### @SATA Cable

Part Number	Description
DC02C007400	H-CONN SET 13D MB-MSATA HDD

### @DC-IN Cable

Part Number	Description
DC30100Q100	CONN SET 13P DCJACK-MB 2DW1003-041110F

### @BATT Cable

Part Number	Description
DC02001X800	H-CONN SET 13D MB-BATT CABLE

### @LED FFC

Part Number	Description
NBX0001JG00	FFC 10P F P0.5 PAD0.3 172MM MB-LED/B 13D

### @FP FFC

Part Number	Description
NBX0001JK00	FFC 8P F P0.5 PAD.3 123MM MB-FP VALIDITY

### @TP FFC

Part Number	Description
NBX0001JJ00	FFC 16P F P0.5 PAD=0.3 119MM MB-TP 13D

### @USH Board FFC

Part Number	Description
NBX0001JJ00	FFC 26P G P0.5 PAD.3 88MM MB-USH/B 13D

### @RTC BATT

Part Number	Description
GC02001D900	BATT CR2032 3V 225MAH PA 5 W/C 30MM

### @FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

### @Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

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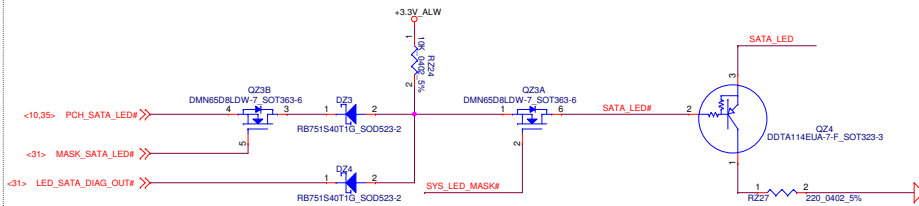
Keyboard

LA-C621P

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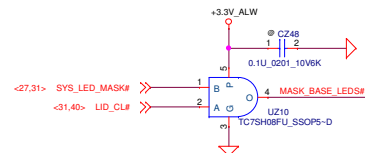
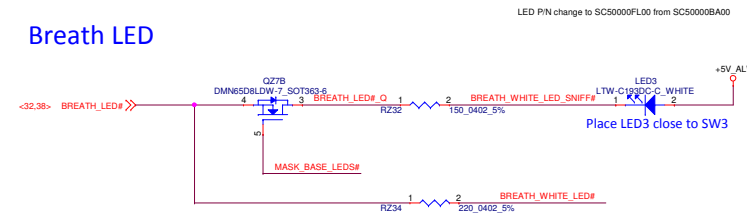
## HDD LED solution for White LED



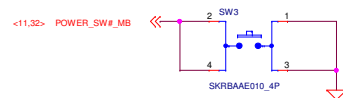
## Battery LED



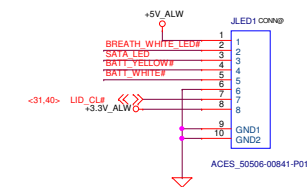
## Breath LED



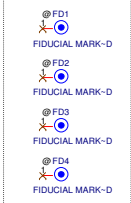
## POWER & INSTANT ON SWITCH



## LED board CONN

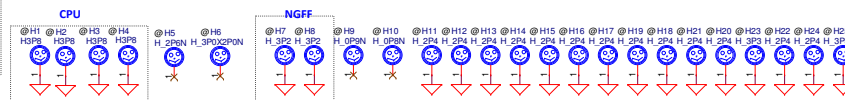


## Fiducial Mark



## LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



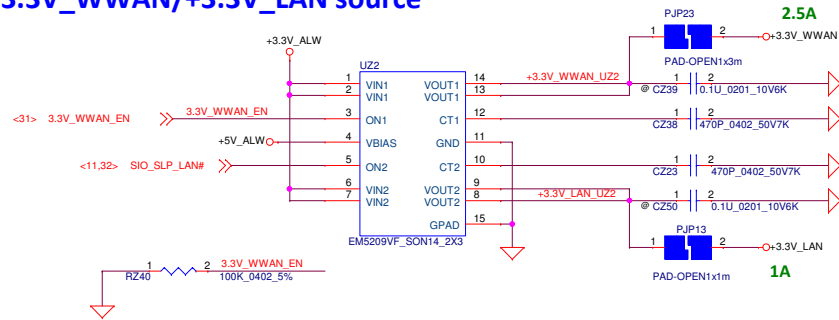
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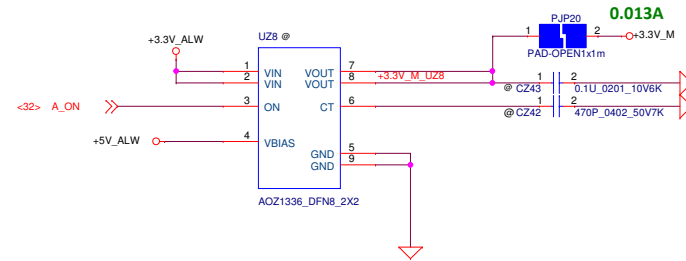
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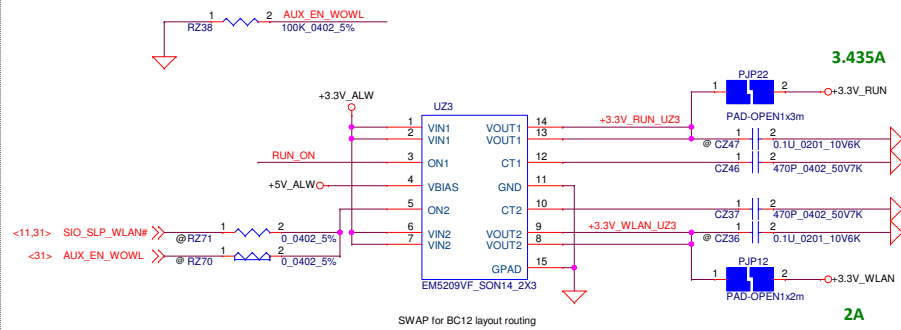
## +3.3V\_WWAN/+3.3V\_LAN source



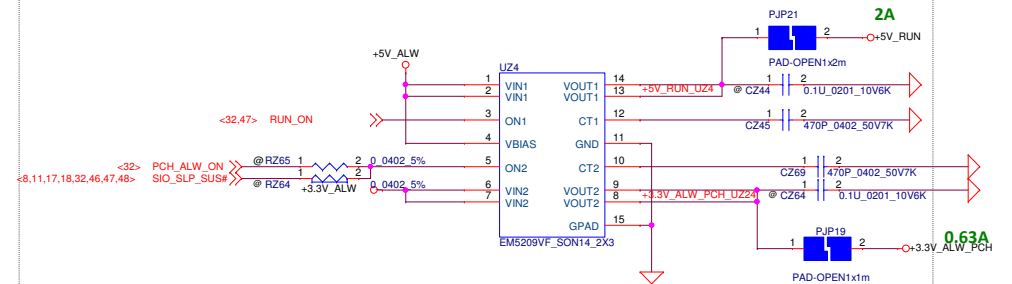
## +3.3V\_M source



## +3.3V\_WLAN/+3.3V\_RUN source



## +5V\_RUN/+3.3V\_ALW\_PCH source



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Power control

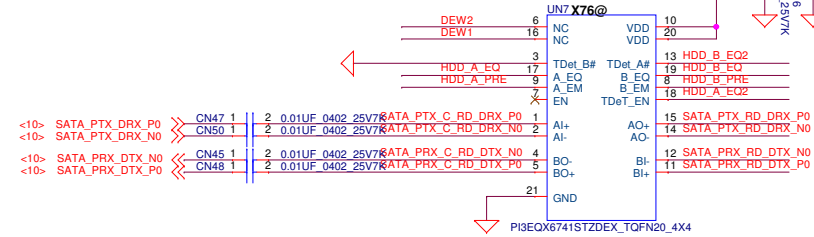
LA-C621P

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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

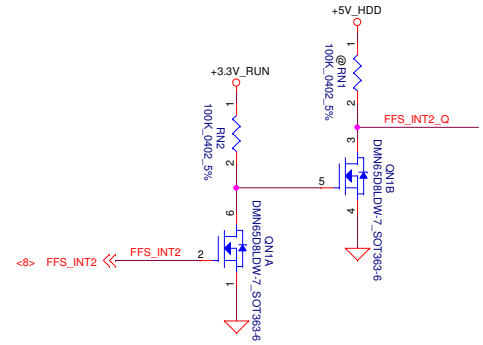
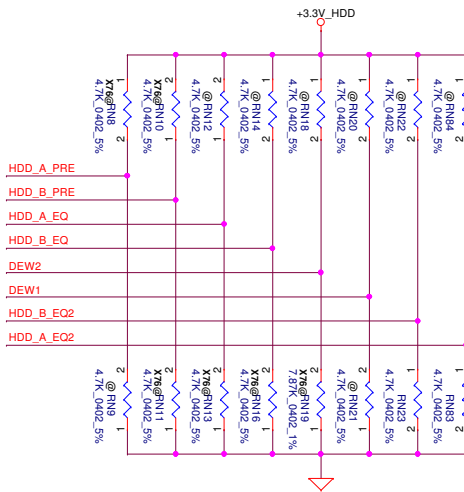
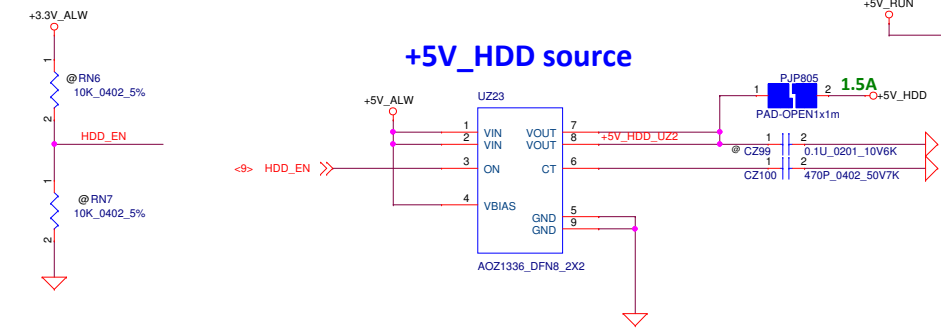
## SATA Repeater



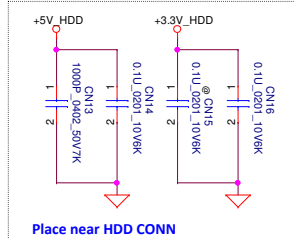
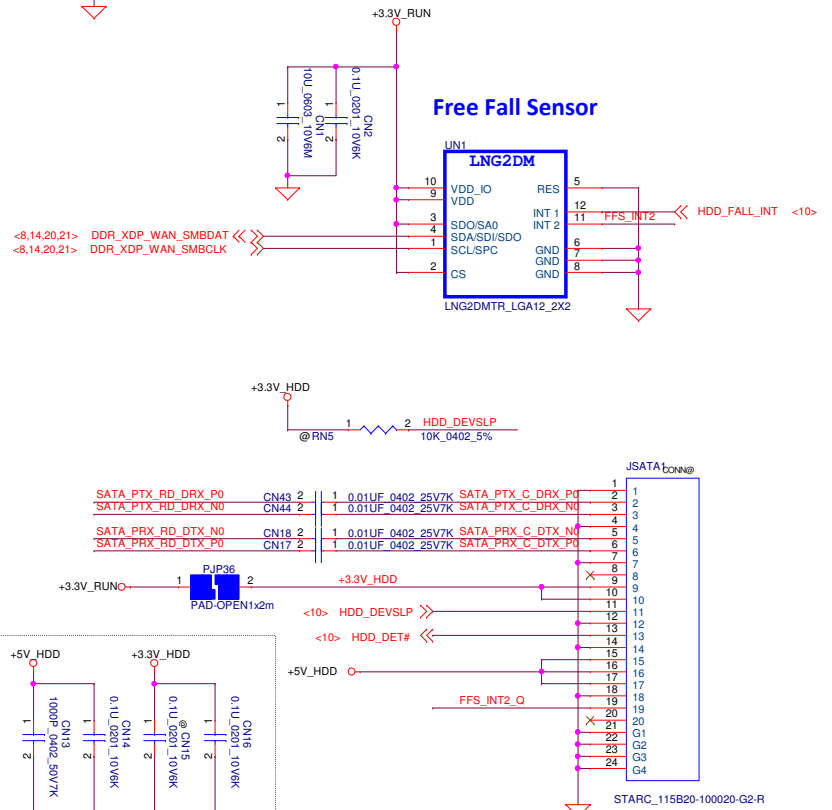
	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	NC	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	NC (IPU)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM	
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB  1.5dB	0dB  1.5dB	
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB	
3rd	Parade	EQ2	EQ1	A_EQ	B_EQ		A_EM	B_EM
		(M = VDD/2)						
		0	M	2.4dB	2.4dB			
		0	0	7.4dB	7.4dB			
		0	1	14.4dB	14.4dB	0	0dB	0dB
		M	M	12.2dB	12.2dB	M	-3.5dB	-3.5dB
		M	0	9.4dB	9.4dB	1	-1.5dB	-1.5dB
		M	1	13.3dB	13.3dB			
		1	M	6.2dB	6.2dB			
		1	0	11.2dB	11.2dB			
		1	1	5dB	5dB			

\* red color is current setting



## Free Fall Sensor

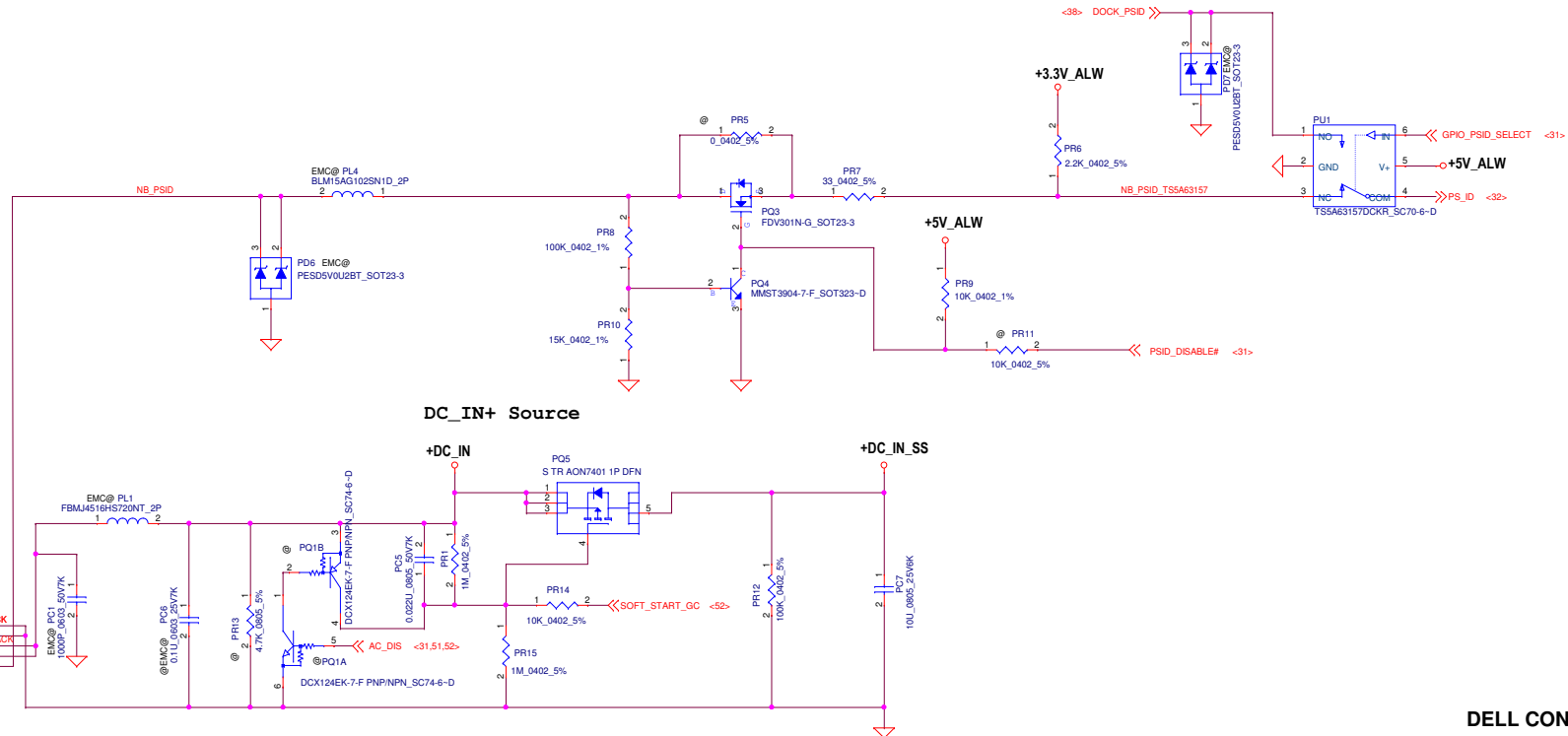
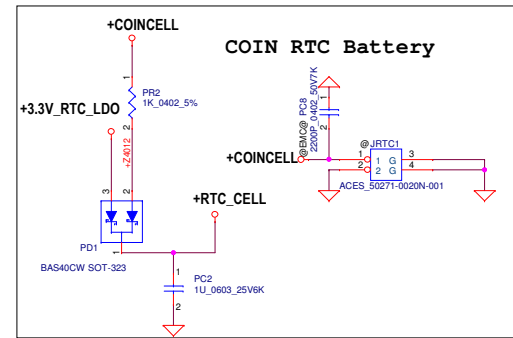
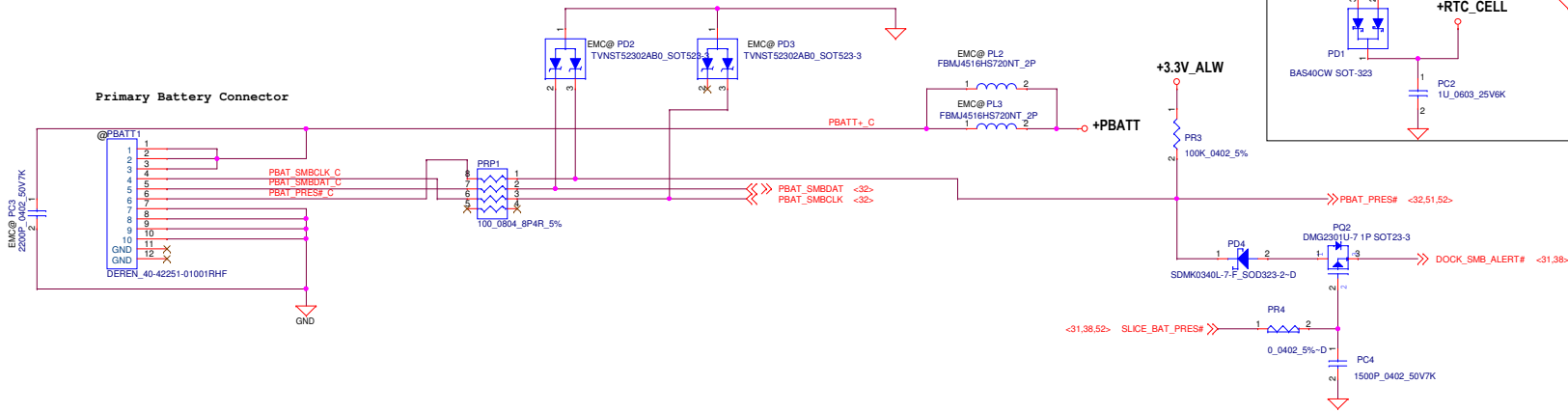


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# Primary Battery Connector

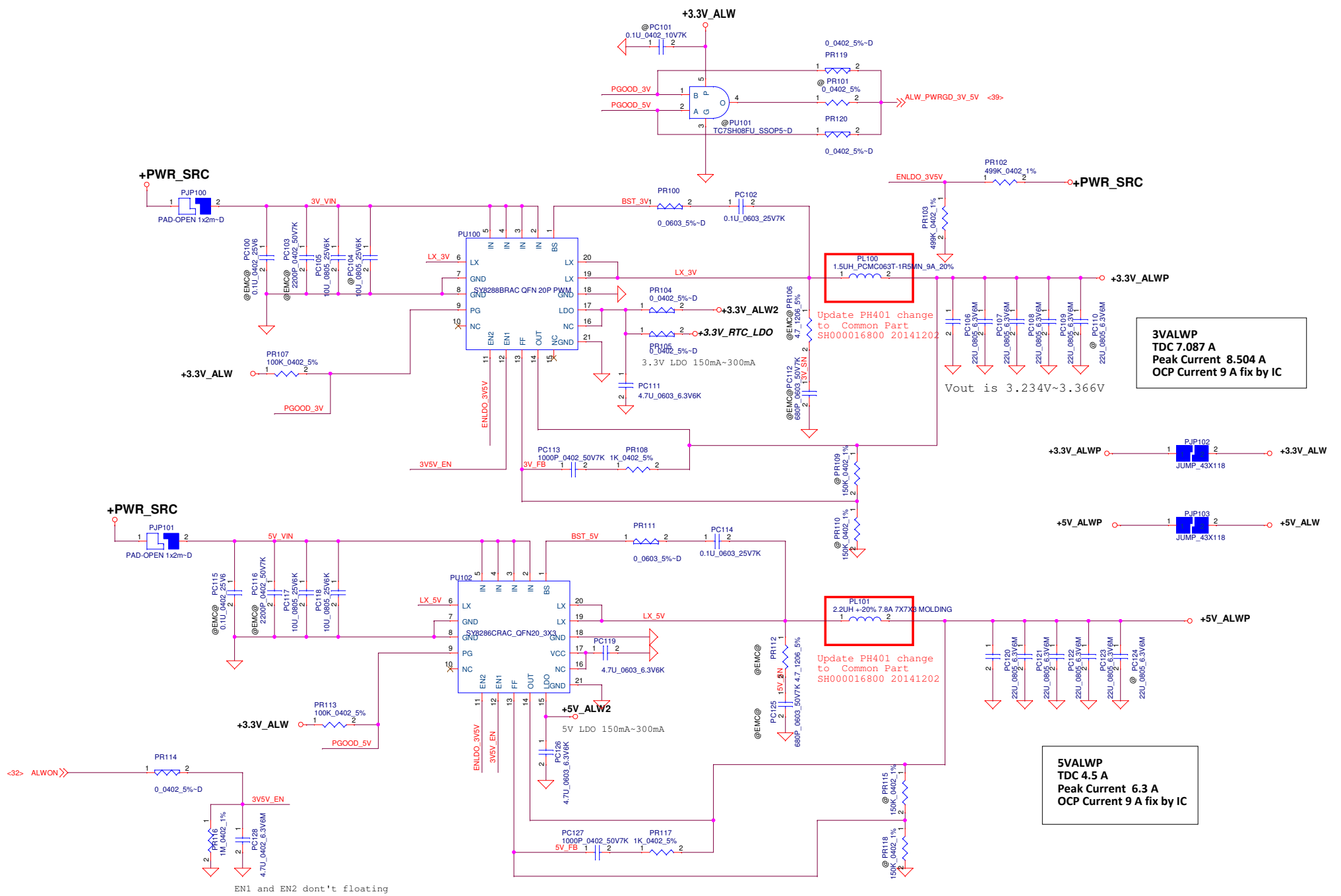


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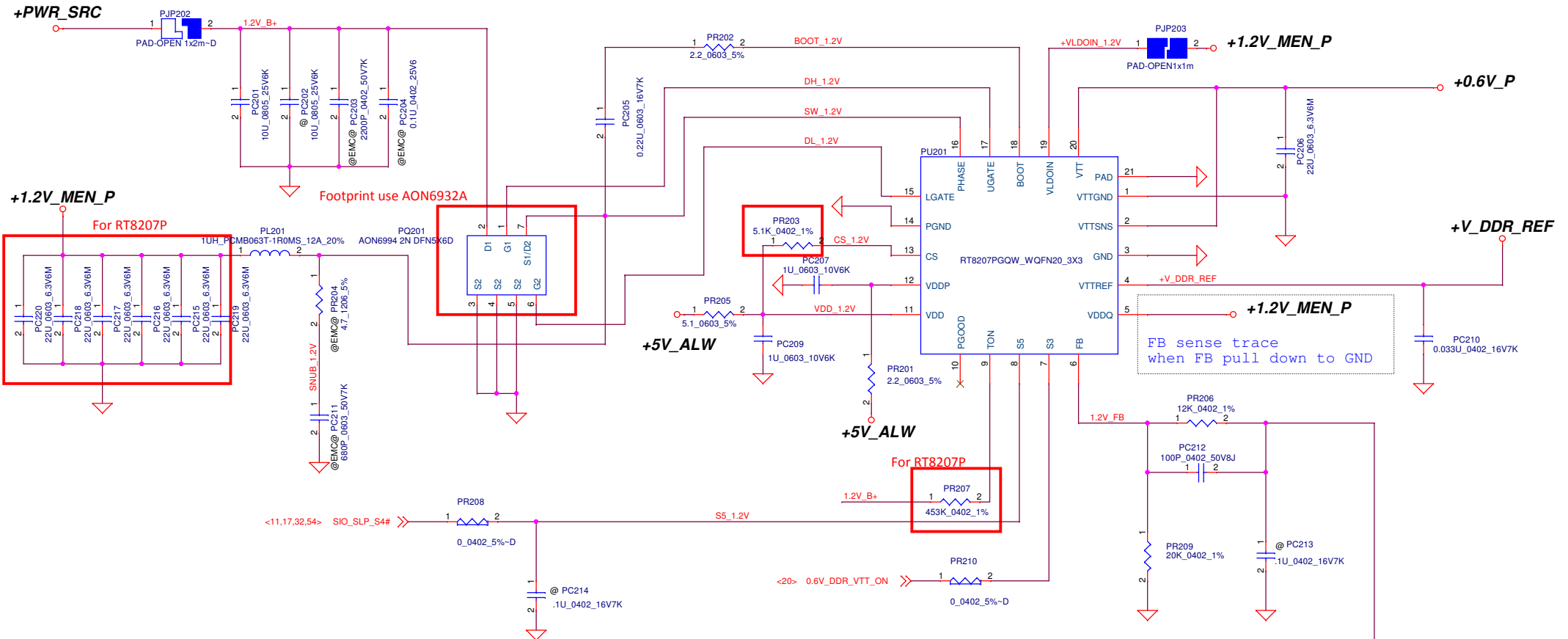


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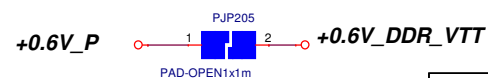
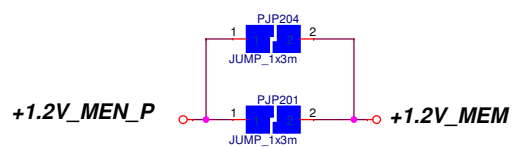
			
<b>Compal Electronics, Inc.</b>			
<b>+5V_ALW/3.3V_ALW</b>			
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0.6Volt +/- 5%  
TDC 0.7 A  
Peak Current 1.0 A  
OCP Current 2.6 A fix by IC



Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

**+1.2V\_MEM**  
**TDC 8.75 A**  
**Peak Current 12.25 A**  
**OCF Current 14.7 A**  
                   **TYP**                  **MAX**  
**H/S Rds(on) 6.7mohm , 8.5mohm**  
**L/S Rds(on) 2.4mohm , 3.2mohm**  
**Choke DCR 3.0mohm , 3.5mohm**  
**CAP ESR 11mohm**



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**Compal Electronics, Inc.**

+1.2V MEN/+0.6V DDR VTT

**LA-C631P, C641P**

Date: Thursday, September 24, 2015

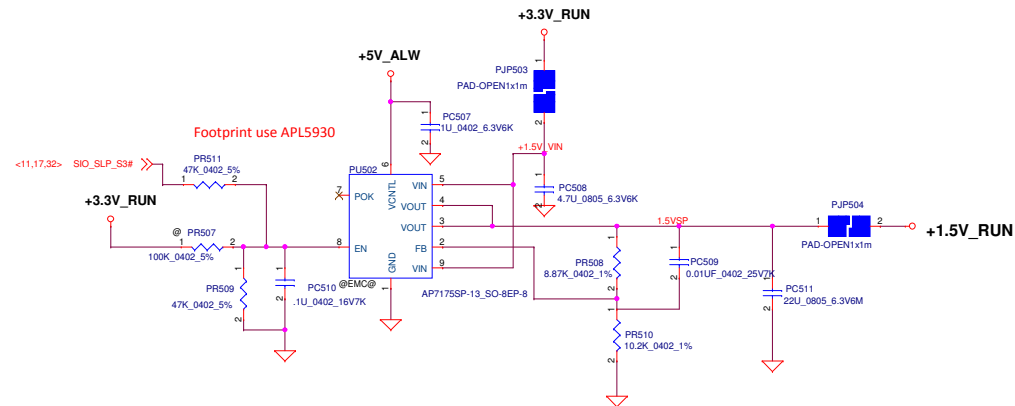
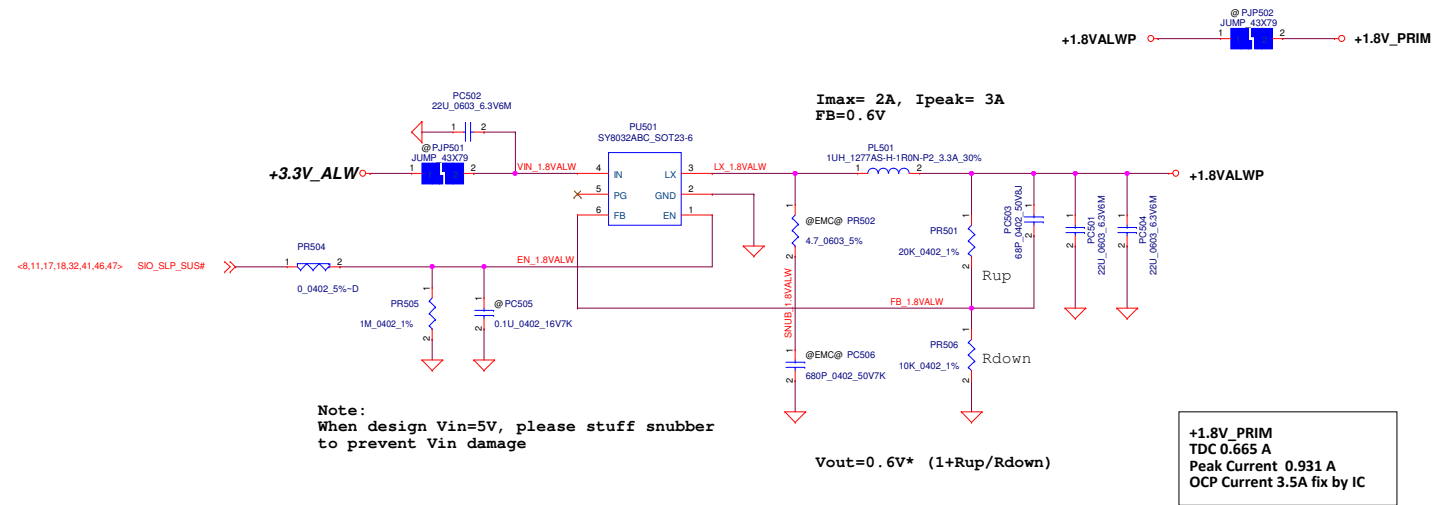
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		+1.8VALWP/+1.5VSP	
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Local sense put on HW site

+1.0V\_VCCST

+5V\_ALW

VCC\_SA  
TDC 3.7A  
Peak Current 4.5A  
OCP current 5.4A  
Choke DCR 13 m ohm

VCCSA\_B+  
CPU\_B+

VCCSA\_B+

+5V\_RUN

+VCC\_SA

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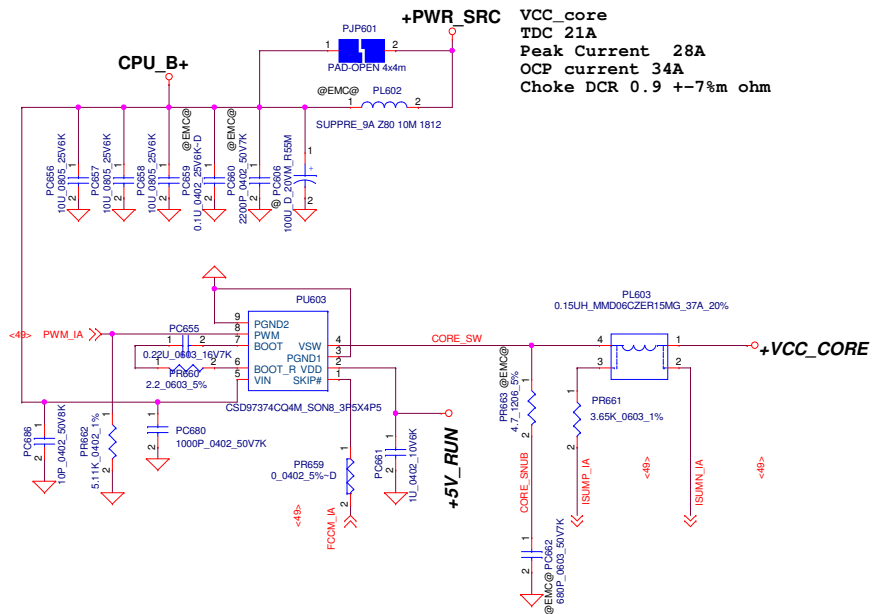
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PWR\_VCORE\_ISL95812 for QC

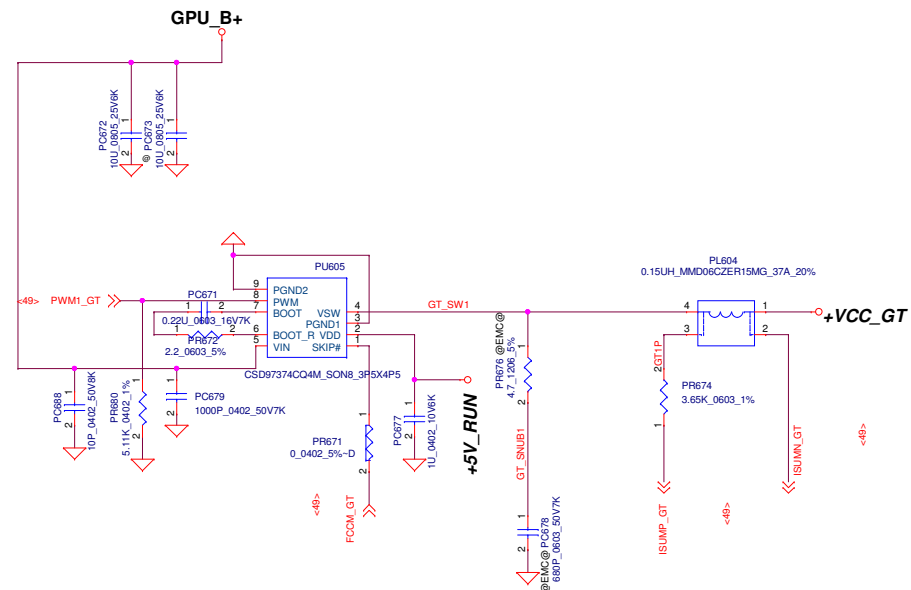
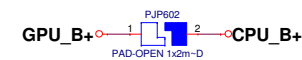
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**VCC\_GT**  
 TDC 18A  
 Peak Current 31A  
 OCP current 37A  
 Choke DCR 0.9 +-7% ohm



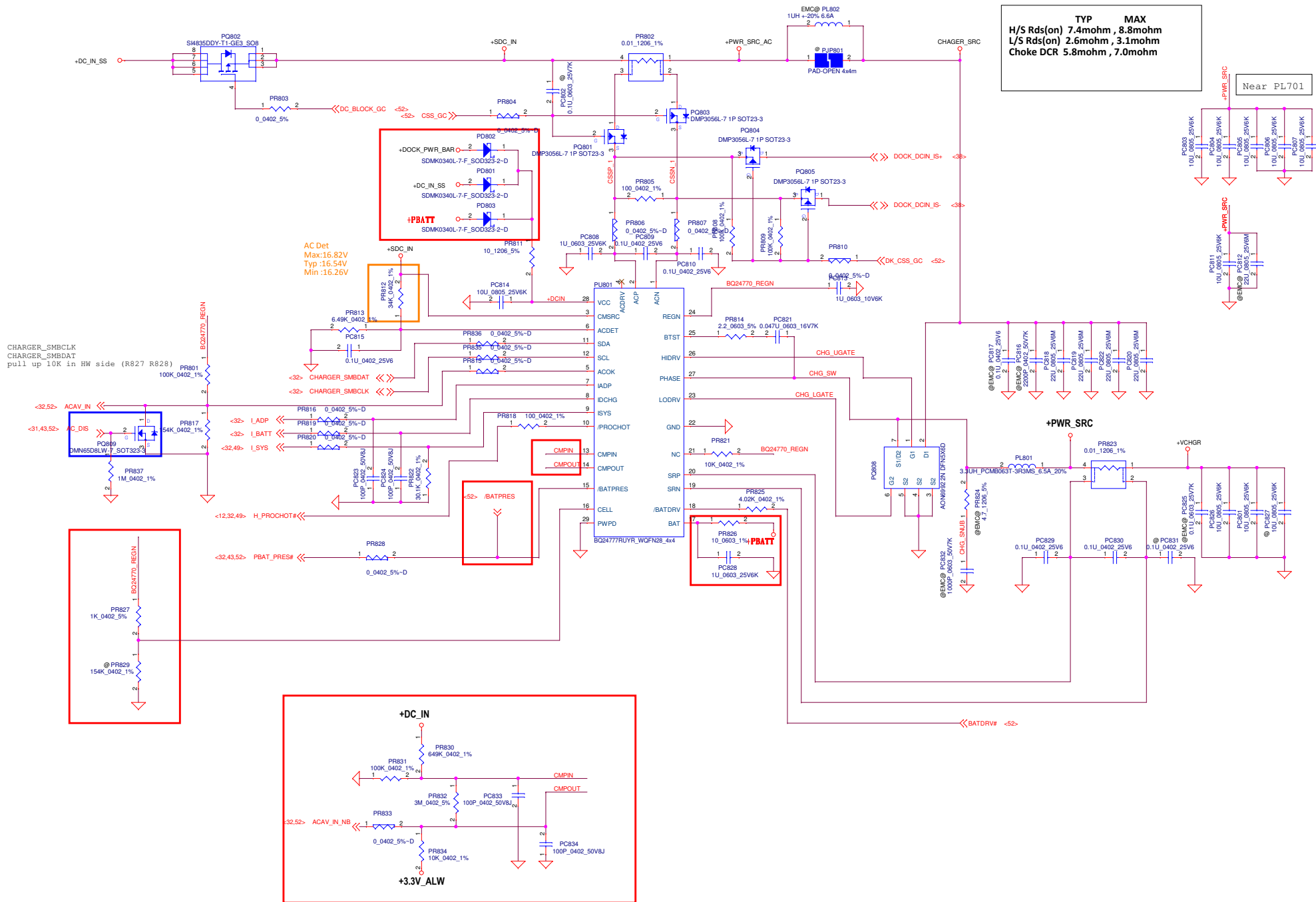
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PWR_VCORE_ISL95812 for QC			
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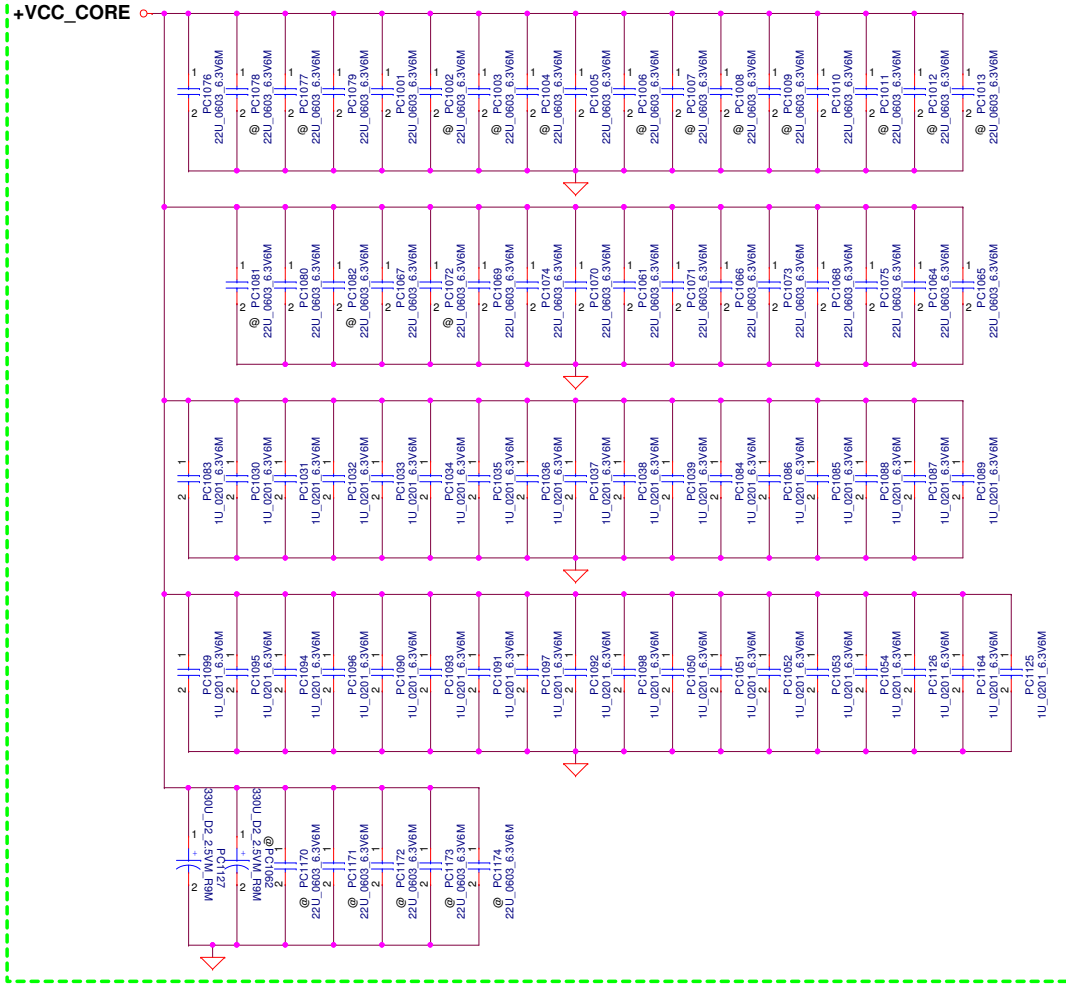
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<b>Charger</b>		<b>LA-C631P, C641P</b>	
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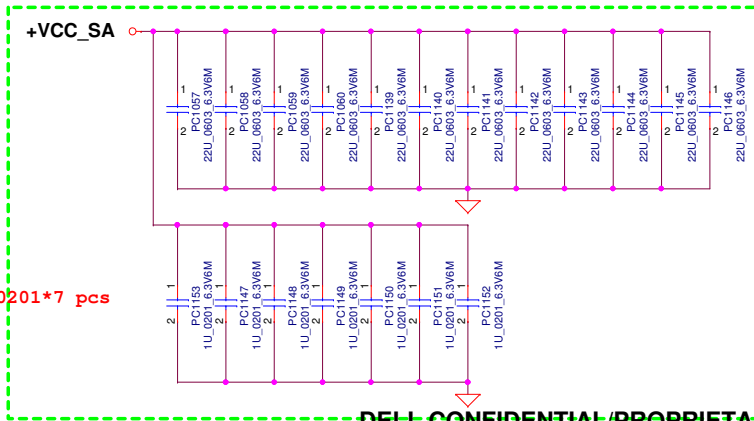
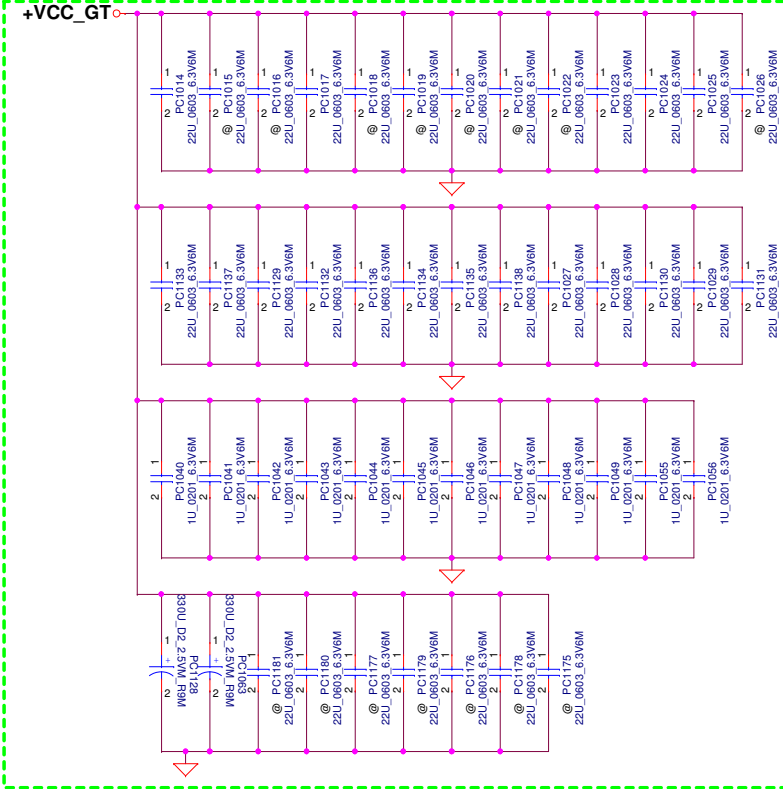


VCC\_CORE Place on CPU  
Back Side.  
22U\_0603 \* 7 pcs +1U\_0201\*35 pcs  
Primary Side.  
22U\_0603 \* 13 pcs+330u\_D2\*1 pcs



VCC\_SA Place on CPU  
Back Side.  
22U\_0603 \* 4 pcs + 1U\_0201\*7 pcs  
Primary Side.  
22U\_0603 \* 8 pcs

VCC\_GT Place on CPU  
Back Side.  
22U\_0603 \* 11 pcs +1U\_0201\*12 pcs  
Primary Side.  
22U\_0603 \* 7 pcs +330u\_D2\*2 pcs

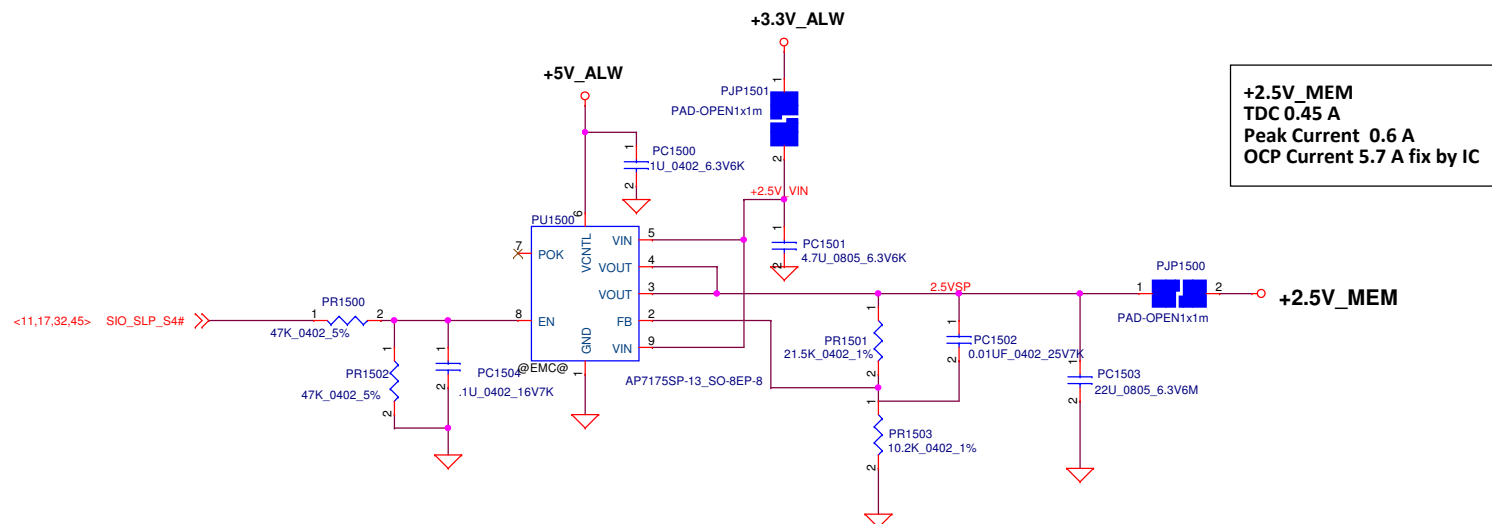


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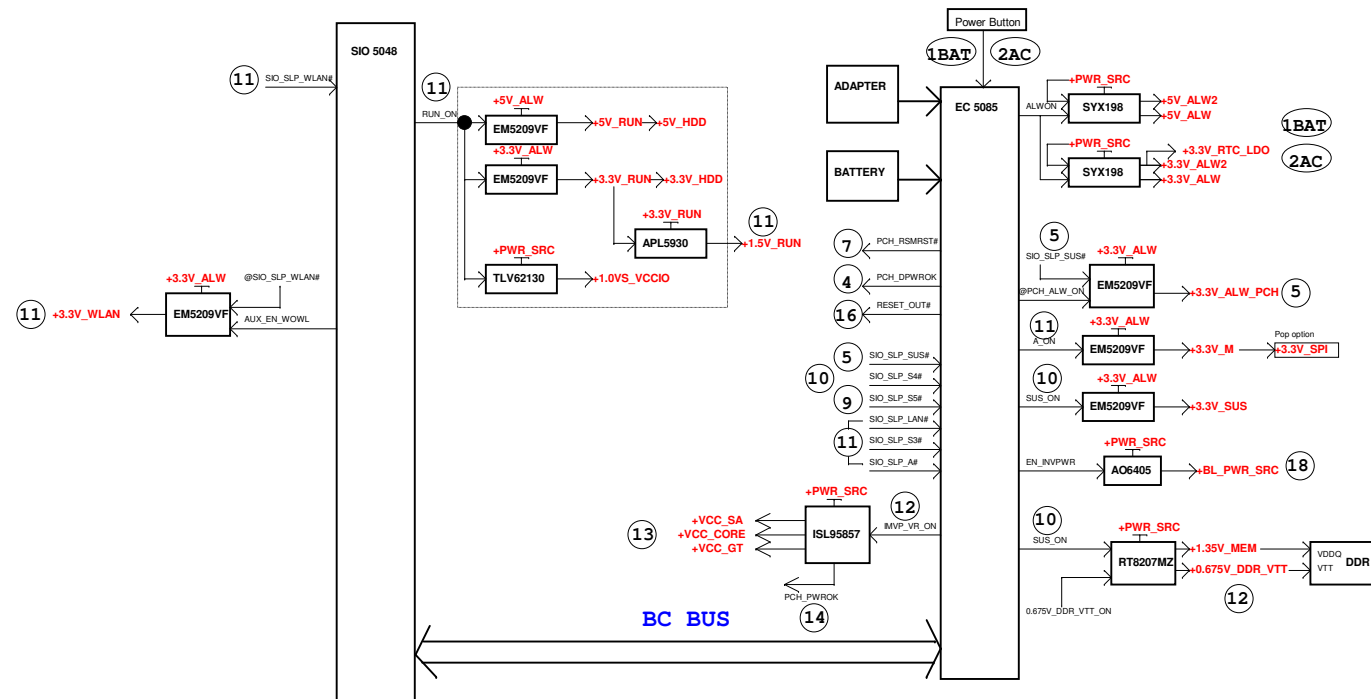
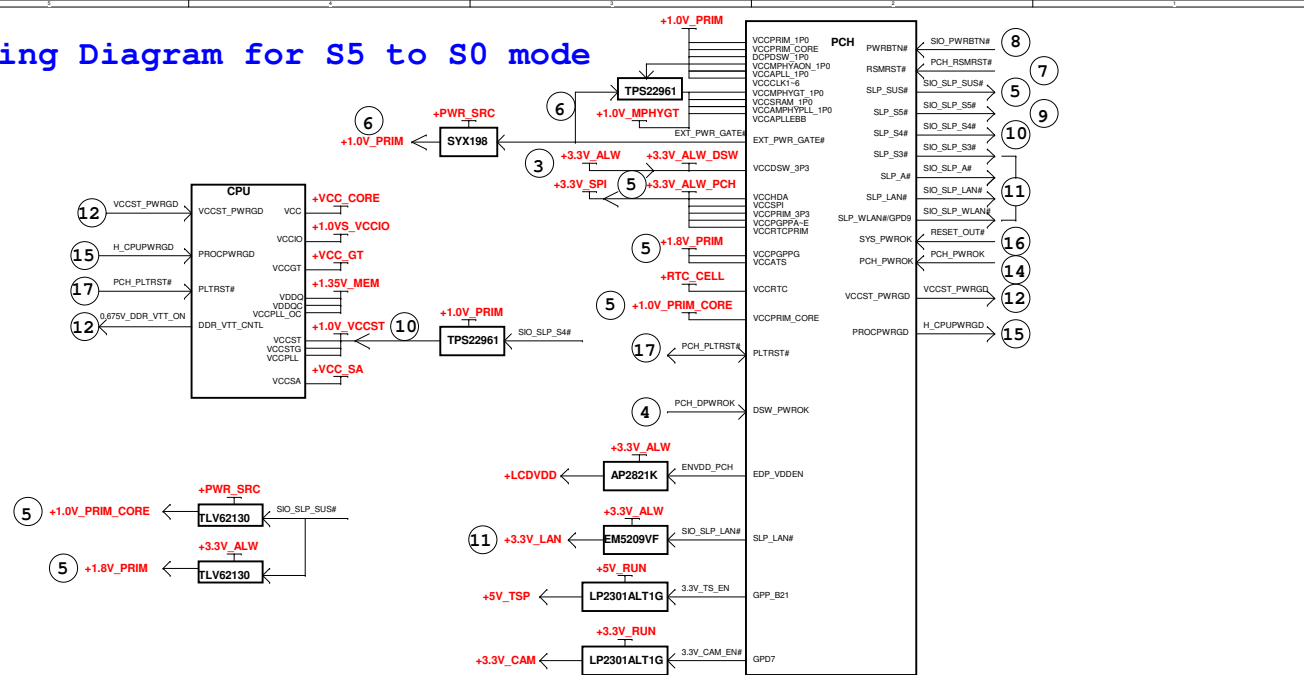


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Title		<b>+2.5V_MEM</b>	
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### Timing Diagram for S5 to S0 mode



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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	VCCIO PRIM_COREP	1/27	Compal	For +1.0VS_VCCIO, +1.0V_PRIM_CORE IC 2nd source	Add PR403, PR406, PR427, PR428	
2	49	+VCC_CORE +VCC_SA +VCC_GT	1/27	Compal	Fine tune IMON	change PR613 to 86.6k change PR651 to 124k change PR629 to 88.7k	
3	49	+VCC_CORE +VCC_SA +VCC_GT	1/27	Compal	Fine tune VR current loop	change PR638 to 374 change PC624 to 0.033uF change PC642 to 0.1uF depop PC646	
4	44	+5V_ALW +3.3V_ALW	1/27	Compal	For 3V5V Pgood	Remove PU101, PR101, PC101 Add PR119, PR120	
5	45	+1.35V_MEM +2.5V_MEM GPU_VRAM	3/3	Compal	For DDR change to DDR3L	Remove +2.5V_MEM, GPU_VRAM power rail circuit change power setting from +1.2 to +1.35	
6	49	+VCC_CORE +VCC_SA +VCC_GT	3/27	Compal	Fine tune VR control loop	change PR640 to 340 change PC642 to 0.033uF change PC646 to 0.047uF change PR657 to 4.42k change PR628 to 4.42k	
7	45	+1.2V_MEM +2.5V_MEM GPU_VRAM	4/10	Compal	For DDR change to DDR4	Add +2.5V_MEM, GPU_VRAM power rail circuit change power setting from +1.35 to +1.2	
8	54	+2.5V_MEM +1.8VALWP +1.5VSP	4/20	Compal	Disable LDO pull up when floating enable pin	change PR1500, PR1502, PR509, PR511 to 47k	
9	51	Charger	4/20	Compal	fine tune monitor Psys	change PR822 to 40.2k	
10		+1VS_VCCIO +1.0V_PRIM_COREP				change to SY80657	
11		CPU MLCC cap cost down			CPU MLCC cap cost down	depop +VCC_CORE, 22U*15, 330U*1 +VCC_GT, 22U*8	

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1	8/22/27/30/40/42	Material	2015/01/05	COMPAL	Material EOL	QA2, QA3, QC2, QE2, QL1, QL2, QN1, QV3, QZ3 and QZ7 from SB00000DH00 change to SB00000ZU00	0.2 (X01)
2	32	MEC5085	2015/01/05	DELL	For Next Gen EC debug	Add Re305 and RE306 reserve UART0_TXD path	0.2 (X01)
3	33	USH & TPM	2015/01/12	COMPAL	system will shut down when insert FP.	change USH conn pin define, and add RZ85, RZ86, DZ7, reserve RZ84, RZ87	0.2 (X01)
4	32	MEC5085	2015/01/12	COMPAL	change BID to X01.	change RE79 to 130K ohm.	0.2 (X01)
5	9	CPU (4/14)	2015/01/12	COMPAL	add UART port 2 for USB debug.	add net name "LPSS_UART2_TXD", "LPSS_UART2_RXD", and add RC330, RC331 and JUART1 CON	0.2 (X01)
6	13	CPU (8/14)	2015/01/12	INTEL	Follow 546765_546765_2014WW52_Skylake_MOW_Rev_1_0	reserve CC222 and RC313.	0.2 (X01)
7	8	CPU (3/14)	2015/01/12	INTEL	support DCI.	add RC327 and reserve RC326, QC3	0.2 (X01)
8	32	MEC5085	2015/01/12	COMPAL	For Power down sequence.	add UE3, UE4, RE304, RE308.	0.2 (X01)
9	11	CPU (6/14)	2015/01/12	COMPAL	For PLTRST glitch issue.	1.UC7.5 change from +3.3V_RUN to +3.3V_ALW_PCH 2.Pop RC325, depop RC60.	0.2 (X01)
10	21	DDR4	2015/01/12	COMPAL	DIMM select error cause can't recognize DIMM2.	Stuff RD70, RD72 and no stuff RD69, RD73.	0.2 (X01)
11	27	Transformer	2015/01/12	COMPAL	ME height limit	TL1 changed from SP050006F00 to SP050006Y00	0.2 (X01)
12	11	Crystal	2015/01/12	TXC	Material EOS	YC2 changed from SJ10000LD00 to SJ10000LV00	0.2 (X01)
13	22	HDMI CONN	2015/01/20	COMPAL	For HDMI EMI solution.	add RV647 ~ RV658 path and depop commom-chock	0.2 (X01)
14	26	LCD	2015/01/20	COMPAL	BOM changed	UV24 from SA00006EE00 to SA00006Y800	0.2 (X01)
15	32	EC	2015/01/20	COMPAL	BOM changed	QE3/QE4/QE5/QE6/QE7 from SB000008P00 to SB000013V00	0.2 (X01)
16	32	EC	2015/01/20	COMPAL	BOM changed	UD1 and UE4 from SA00005U600 to SA00007UR00	0.2 (X01)
17	33	TPM	2015/01/20	COMPAL	TPM issue	1. Reserve10K ohm (RZ90) and Pull-up to +3.3V_RUN on UZ12 pin 29. 2. change VSB power (UZ12.1) to +3.3V_ALW_PCH. 3. added QZ8 and RZ109 between pin3/pin20 to control LPM 4. reserve RZ110 and de-pop. 5. Reserve +3.3V_RUN on UZ12 pin 8 (add RZ88, RZ89) 6. change RZ109 pin lto +3.3V_M_TPM add QZ9, RZ111	0.2 (X01)
18	9	CPU (4/14)	2015/01/20	COMPAL	Non-Dock config	Reserve RH359 pull-down for non-dock config	0.2 (X01)
19	32	EC	2015/01/20	COMPAL	Power sequence fail	Depop RE280 and RE304 then pop RE292 and UE3	0.2 (X01)
20	18	CPU (13/14)	2015/02/04	COMPAL	KB boss and stand off interference	Removed RC304/RC305/RC306/CC205/CC207/CC265	0.3 (X02)
21	10	CPU (5/14)	2015/02/04	INTEL	MOW update	Add RC337 connect to GND and RC338 1K pull down	0.3 (X02)
22	12	CPU (7/14)	2015/02/04	INTEL	MOW update	Add RC328 XDP_JTAGX need connect to CPU_XDP_TCLK for DCI	0.3 (X02)
23	8	CPU (3/14)	2015/02/04	INTEL	MOW update	Changed RC317 from 4.7k to 150k and reserved SIO_SLP_SUS# on RC340	0.3 (X02)
24	20, 21	DDR4	2015/02/04	INTEL	Follow 546765_546765_2015WW02_Skylake_MOW_Rev_1_0	No stuff CD6, CD35.	0.3 (X02)

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Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
25	33	USH & TPM	2015/03/02	Nuvoton	1.for allow further reducing power in TPM 2.0 F/W,when system is in S3/4/5 and main power is off. 2.for support modern standby.	1.reserve RZ90 2.reserve RZ112. 3.Depop RZ88 and pop RZ89, pop RZ112	0.3 (X02)
26	11,27	CPU (6/14)	2015/03/02	COMPAL	Solve auto power on issue.	De-pop RL70 and pop RC323.	0.3 (X02)
27	32	MEC5085	2015/03/02	COMPAL	Solve power down sequence fail.	De-pop RE308.	0.3 (X02)
28	32	MEC5085	2015/03/02	COMPAL	change BID to X02.	change RE79 to 33K ohm.	0.3 (X02)
29	26	eDP CONN & TS	2015/03/02	DELL	Customer request.	add 6 pin IR Conn.	0.3 (X02)
30	40	PAD, LED	2015/03/02	COMPAL	ME design change.	change H6 from 4mm to 3mm.	0.3 (X02)
31	11/32	Crystal	2015/03/02	COMPAL	X'tal EA measurement.	change CC23 and CC26 from 18pf to 12pf	0.3 (X02)
32	8	CPU (3/14)	2015/03/02	Intel	Intel MOW_2015WW06:Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update	de-pop RC30, RC316	0.3 (X02)
33	8	CPU (3/14)	2015/03/02	COMPAL	Follow CRB setting	RC23 changed from 8.2K to 2.2K	0.3 (X02)
34	33	TPM	2015/03/02	COMPAL	support modern standby	Add RZ112 connect to SIO_SLP_S0# with TPM	0.3 (X02)
35	32	EC	2015/03/02	COMPAL	Option DDR3L and DDR4	Add GPP_D9(DIMM_TYPE), RC342 and RC341 that selected DDR3L and DDR4.	0.3 (X02)
36	32	EC	2015/03/02	COMPAL	Follow Intel power sequence	Pop RE292 and depop RE280	0.3 (X02)
37	8	CPU (3/14)	2015/03/02	COMPAL	RF request	Pop CC3/CC4/CC5/CC6 from 22p to 27p	0.3 (X02)
38	33	TPM	2015/03/02	Nunoton	TPM detected sequence	Add RZ113 100 ohm	0.3 (X02)
39	11	CPU (6/14)	2015/03/02	COMPAL	Deep S3 leakage	VRLERT# changed power rail from +3.3V_ALW to +3.3V_ALW_PCH	0.3 (X02)
40	27	LAN	2015/03/02	COMPAL	IEEE EA measurement.	change LL2 ~ LL9 to 2.2 ohm Res (RL71~RL78).	0.3 (X02)
41	9	CPU (4/14)	2015/04/02	COMPAL	IR Function	1.add IR_CAM_DET# on JIR1 pin 1. 2.add IR_CAM_DET# on UCL.AW7, and PU 100K(RC346) to +3.3V_RUN	0.4 (X03)
42	31/33	EC/USH	2015/04/02	Broadcom	Vender recommend	1.Reserve RZ114/RZ115 on JUSH1 pin 21 2.add USH_RST# on UE1.A62	0.4 (X03)
43	12	CPU (7/14)	2015/04/02	COMPAL	SIO_EXT_SMI# to wake up system when non-deep S3	Add RC236 SIO_EXT_SMI# change power to +3.3V_ALWS_PCH	0.4 (X03)
44	29	NGFF Card	2015/04/02	COMPAL	ME request	Change JSIM1 conn to T-SOL_5-991503004000-6	0.4 (X03)
45	32	MEC5085	2015/04/02	COMPAL	change BID to X03	change RE79 to 1K ohm.	0.4 (X03)
46	9	CPU (4/14)	2015/04/02	COMPAL	for DIMM type option	Pop RC342 and de-pop RC341	0.4 (X03)
47	40	PAD, LED	2015/04/02	COMPAL	ME request	Add H9 and H10 for different SIM CON	0.4 (X03)
48	29	NGFF	2015/04/02	COMPAL	SIM detect	Add RI31 connecting with JSIM1.9 and NGFF2.58	0.4 (X03)
					<div> <div>  <div> <div>DELL CONFIDENTIAL/PROPRIETARY</div> <div>Compal Electronics, Inc.</div> <div>EE P.I.R (2/3)</div> <div>LA-C621P</div> <div>Thursday, September 24, 2015</div> <div>Sheet 58 of 60</div> </div> </div> </div>		


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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
49	39	KB	2015/04/20	ALPS	For new U1 TP module	Add RZ116 and RZ117 PU on I2C._1_SDA_R/I2C_1_SCL_R	0.4 (X03)
50	31	5048	2015/04/20	COMPAL	PC common EC code issue need reserved PU	Add AR_SMBUS_ALERT# 10K(RE309) PU on ECE5048 pin58 GPIOF2	0.4 (X03)
51	31	All	2015/04/20	COMPAL	Changed 0 ohm short-pad	R274, RA35, RA36, RA37, RC143, RC169, RC170, RC171, RC172, RC173, RC211, RC214, RC228, RC229, RC230, RC231, RC235, RC290, RC295, RC296, RC299, RC300, RC301, RC302, RC303, RC307, RC308, RC309, RC310, RC325, RC327, RC328, RC337, RC37, RD29, RD60, RD65, RD66, RD67, RD68, RD70, RD72, RD74, RE290, RE305, RI15, RI16, RI17, RI18, RI19, RI20, RI21, RI22, RI23, RI24, RI25, RI26, RI27, RI28, RI29, RI30, RI31, RL34, RL7, RN99, RR17, RR18, RR21, RR22, RR23, RZ22, RZ23, RZ56, RZ70, RZ85, RZ86	0.4 (X03)
52	8	CPU(3/14)	2015/04/20	COMPAL	SMBUS LAN backdrive	Add RC347 and RC348 PU to +3.3V_ALW_PCH	0.4 (X03)
53	11	CPU(6/14)	2015/05/20	COMPAL	Crystal EA -R issue	Changed YC2-CL 9pf from 12pf and cc23/cc26 changed to 6pf from 12pf	0.5 (X04)
54	35	M2280	2015/05/20	COMPAL	Insert NVME SATA LED no function	JNGFF3.10 connected to PCH_SATA_LED#	0.5 (X04)
55	36	USB	2015/05/20	COMPAL	Insert Storage Bus shutdown	Add CI32 150U prevent charger current over spec	0.5 (X04)
56	39	TP	2015/05/20	COMPAL	TP function sometimes lag or crazy	CZ30 and CZ31 change from 10p to 330p improve signal quality	0.5 (X04)
57	31	5048	2015/05/20	COMPAL	For Type-C function	1. Add 5048 GPIO(PROCHOT_GATE) and reserve RE311 pull high 2. Add 5048(PD_ACE_DET#) for AR config and pull high on RE310	0.5 (X04)
58	32	MEC5085	2015/05/20	COMPAL	change BID to X04	change RE79 to 8.2K ohm.	0.5 (X04)
59	18	CPU(13/14)	2015/05/27	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	1.Add RC349 and CC303 on VCCHDA 2.Add RC350 and CC304 on VCCAPLL_1P0	0.5 (X04)
60	36/37	USB3.0	2015/05/27	COMPAL	ESD request	1.Add CI33 0.1U cap to GND on USB_OC0# 2.Add CI34 0.1U cap to GND on USB_OC1# 3.Add CI35 0.1U cap to GND on USB_OC2#	0.5 (X04)
61	26	eDP	2015/06/27	COMPAL	Material shortage	Changed DV1, DV2 and DV3 from SCS00003800 to SCS00006400	0.6 (X05)
62	33	TPM	2015/06/27	COMPAL	Change TPM FW to 1.2 version	Changed UZ12 from SA000082D00 to SA00008EL20	0.6 (X05)
63	32	KBC	2015/06/27	COMPAL	WinPE Global reset shutdown issue	Add QE11 prevent +1.0V_VCCST timing down before +1.0V_VCCIO	0.6 (X05)
64	32	KBC	2015/06/27	COMPAL	Follow intel power sequence	Add UE5 AND Gate control Run_on timing and depop RE292	0.6 (X05)
65	11	CPU(6/14)	2015/06/27	COMPAL	Cystal EA	Changed CC21 and CC22 from 22p to 15p	0.6 (X05)
66	33	USH	2015/06/27	COMPAL	TPM1.2 deep S3 resume issue	UZ12.1 changed power rail from +3.3V_ALW_PCH to +3.3V_ALW	0.6 (X05)
67	24	DP HUB	2015/07/20	COMPAL	For DP hub display flicker issue	1.Add UV29, CV617, CV618, CV619, RV659, RV650, RV661 2.Depop UV28, PJP33, CV615, CV616	0.6 (X05)
68	36	HW	2015/07/20	COMPAL	For Sourcer request	CI32 change from SGA00002N80 to SGA00004E10	0.6 (X05)
69	32	MEC5085	2015/07/20	COMPAL	change BID to X05	change RE79 to 4.3K ohm.	0.6 (X05)

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Title <b>EE P.I.R (3/3)</b>							
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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Owner	Issue Description	Solution Description	Rev.
70	41	CPU(12/14)	2015/07/31	COMPAL	Follow Intel DG1.5	Add load switch (UZ26) control to +VCCPLL_OC power rail	0.6(X05)
71	18	CPU(13/14)	2015/07/31	COMPAL	5.76GHz noise observed on thie Wi-Fi antenna	Change RC349 and RC350 to LC1 and LC2	0.6(X05)
72	36	USB	2015/08/12	COMPAL	Low battery shut down issue	Depop CI32 and then pop CI14	0.6(X05)
73	32	5085	2015/08/12	COMPAL	DC mode CPU trubo issue	Reserved RE313 pull down path on I_SYS	0.6(X05)
74	34	PCIE	2015/08/12	COMPAL	M.2 SATA iEMT	Pop RN50 change to level2	0.6(X05)
75	11	CPU(6/14)	2015/08/12	COMPAL	RTC delay	YC2 changed to 10ppm(SJ10000Q800) and CC23/CC26 changed to 5pf	0.6(X05)
76	24	HUB	2015/09/12	COMPAL	Display no function	RV662 chnanged to 0 ohm from 1 ohm.	1.0(A00)
77	ALL	All	2015/09/12	COMPAL	Changed 0 ohm short-pad	RC41,RC289,RZ89,RZ112,RZ64,RC221,RZ118,RV662	1.0(A00)
78	12	CPU(7/14)	2015/09/12	COMPAL	Service mode switch	Depop RC222 and SW1 and then short RC221	1.0(A00)
79	32	5085	2015/09/12	COMPAL	syn-up with power material issue	1.Change SC600001600 to SCA00000T00 (DI2,DI3,DI5,DV4) 2.Change SB0000013V00 to SB000000Z500 (QE3,QE4,QE5,QE6,QE7)	1.0(A00)
80	32	MEC5085	2015/09/12	COMPAL	change BID to A00	change RE79 to 1K ohm.	1.0(A00)
81	22	HDMI	2015/09/18	COMPAL	DFX request	Delete LV3/LV6/LV9/LV12 co-lay footprint	1.0(A00)
82	12/14	XDP	2015/09/20	COMPAL	Follow PDG2.0	Changed RC82 and RC135 to 100 from 51.	1.0(A00)
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